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# A METHOD OF DESIGNING AVALANCHE TRANSISTOR TRIGGER CIRCUITS

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## SUMMARY

The operation of transistors in the avalanche mode provides a simple but effective means for generating fast pulses. With present transistors there is a large spread of avalanche voltage between individual specimens, and the paper describes a method of designing trigger circuits which require no adjustment when transistors are changed.

Some selection of transistors is necessary for fast operation, and it was found that of the transistors tested, which had $\alpha$ cut-off frequencies in the region of 10 Mc/s, about 20% had avalanche rise times less than 10 millimicrosec, 10% less than 3 millimicrosec, and 5% less than 1·5 millimicrosec. Circuits are described for generating pulses with rise times of 1 millimicrosec and having any width from 1 millimicrosec to several microseconds at half height.

The collector current of an avalanching transistor may build up to 0·5 amp in a few millimicroseconds and no suitable diodes have been found for shaping such waveforms. However, good results have been obtained by using the non-linear capacitance of diodes biased in the reverse direction.

Particular attention is paid to threshold stability and the generation of pulses accurately delayed in relation to the trigger pulse.

An example of a practical application of these circuits is a wide-band oscillograph described in Reference 8.

## LIST OF SYMBOLS

$\alpha$ = Normal transistor current gain.
$C$ = External added capacitance.
$C_c$ = Collector depletion-layer capacitance.
$G$ = Loop gain = $M\alpha$.
$G_1$ = Loop gain in region I.
$G_2$ = Loop gain in region II.
$I_c$ = Defined collector current.
$I_e$ = Defined emitter current.
$I_b$ = Defined base current.
$I_0$ = Initial triggering current.
$i_{co}$ = Collector reverse leakage current.
$M$ = Avalanche multiplication factor.
$M_{eff}$ = Effective avalanche multiplication factor.
$M_1$ = Assumed multiplication factor when $|v_c| > V_x$.
$V_A$ = Avalanche voltage.
$V_c$ = Collector voltage.
$V_p$ = Punch-through voltage.
$V_x = 0{\cdot}97V_a$.
$v_c$ = Instantaneous collector voltage.
$(dv_c/dt)_2$ = Rate of rise of $v_c$ in region II.
$T_0$ = Transistor dispersive transit time.

## (1) INTRODUCTION

The operation of transistors in the region where avalanche multiplication occurs within the collector depletion layer is now reasonably well understood,[1,2] and some practical circuits have been described.[3,4,5]

At the time of writing, no avalanche transistors are commercially available as such, but suitable transistors may be selected at a reasonable yield rate from batches of ordinary medium-frequency transistors. As the transistors thus selected have not been designed specifically for avalanche operation, large variations in parameters are encountered between units. It is the aim of the paper to describe a method of designing trigger circuits which are relatively insensitive to these variations.

The characteristics of the avalanche mode of operating junction transistors are qualitatively identical with those of the point-contact transistor. Thus, many of the trigger circuits which have been designed for point-contact transistors (for example, References 6 and 7) can be directly applied to avalanche operation if allowance is made for the quantitative differences between the two devices. However, it is not the purpose of the paper to catalogue the numerous circuit configurations which follow from this similarity, but to discuss the design of a basic circuit for generating very short pulses.

The generation of high-power pulses of one or two millimicroseconds duration, especially if they can be very accurately timed with reference to some preceding event, is of great value in developing general high-speed switching circuits. Amongst the many other applications of short pulses is the use of sampling techniques in which the amplitude of an input waveform is sampled at discrete points by the pulse, the resulting information being processed at leisure. In such cases the resolution or 'rise time' of the system is determined simply by the pulse width.

Bistable circuits have been excluded since, in general, there is excessive power dissipation on the 'on' state. A further difficulty arises from the fact that capacitive feedback arrangements for the attainment of a fast rise may result in instability.

## (2) AVALANCHE TRANSISTOR CHARACTERISTICS

In avalanche operation, collector voltages in excess of normal operating voltages are applied to a junction transistor so that the electric field within the collector depletion layer is much greater than the normal value. If the electric field is large enough, holes diffusing across the base from the emitter region are accelerated to high velocities on entering the depletion layer, and enough energy may be imparted to them to generate further hole-electron pairs by collision within the crystal structure. Owing to the high field, the holes so generated drift rapidly into the collector region, and the associated electrons drift in the opposite direction to the base. If the electric field is high enough, the secondary holes may be accelerated sufficiently to cause further ionization by collision, and the process may be continued with the net result that, for each hole crossing the base layer from the emitter, a large number may enter the collector region. It will be noted that the mechanism is rather similar to that of multiplication in gases.

The effect of avalanche multiplication on the common-base characteristics of a transistor is shown in Fig. 1. At low collector voltages the field at the collector junction is not high enough to give rise to multiplication, and the normal characteristics are observed. However, as the collector voltage increases, the multiplication effect becomes evident and the collector current

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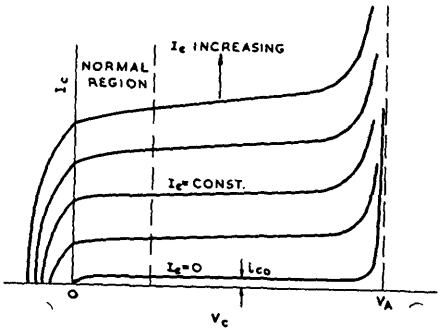



Fig. 1.—Common-base characteristics.

rises rapidly, even though the emitter current is held constant, until eventually a point is reached where complete breakdown occurs and very high values of collector current are attained. At this point, it is found that a large collector current can be maintained, even when the emitter current is zero. In this case, the current carriers which enter the depletion layer and become multiplied to make up the total collector current are, in fact, merely thermally generated minority carriers, which at low collector voltage are recognized as $i_{co}$.

The multiplication at the collector junction gives rise to a substantial increase in the effective current gain of the device at voltages near the breakdown region, as shown by the increase in spacing between curves for constant $I_e$ in Fig. 1. The current gain is then $M\alpha$, where $\alpha$ is the normal current gain at low collector voltage, and $M$ is the multiplication factor.

It has been found empirically[1] that the multiplication can be expressed by $M = 1/[1-(V_c/V_A)^3]$ for germanium-alloy junction transistors, where $V_c$ is the collector voltage and $V_A$ is the voltage at which complete breakdown occurs.

$V_A$ is determined mainly by the doping of the base material. In an alloy junction transistor the impurity concentration is much lower in the base region that in the collector region, and thus nearly all the depletion layer is on the base side of the collector junction. At any given collector voltage, the depletion layer must contain just enough donor centres (which possess a fixed positive charge) to produce an electric field which exactly neutralizes the externally applied field at the base edge of the depletion layer. If the base region contains a large number of such donor centres (i.e. if it is of high conductivity), the depletion layer need only be very narrow to satisfy this condition, and the potential gradient within the region is thus very high. In such a case, a small applied voltage may be sufficient to raise the electric field to breakdown strength. In a base region of low conductivity, however, the depletion layer becomes much wider at a given applied voltage in order to include the necessary number of donor centres, and to produce the potential gradient required for breakdown a much larger voltage must be applied to the collector.

If the conductivity of the base material is too low, or if the base region is very narrow, a situation may arise where the collector depletion layer extends completely across the base region without the occurrence of avalanche breakdown. This condition is known as 'punch-through', and the voltage required to arrive at it is the punch-through voltage $V_p$.

Avalanche transistors are selected so that $V_A$ is less than $V_p$, but close to it. In an avalanche transistor of properly chosen base conductivity and dimensions, the depletion layer extends across most, but not all, of the base region at collector voltages near $V_A$, so that the active width, i.e. the portion of the base between the emitter junction and the edge of the collector depletion layer, is only a fraction of the total width of the base material. The transit time of carriers from emitter to collector is thus greatly reduced [since, in the diffusion process, transit time is proportional to (base width)$^2$] and the effective cut-off frequency is increased considerably. Thus, in a suitable transistor, the application of collector voltages approaching $V_A$ can result in (*a*) an increase in current gain to many times greater than unity and (*b*) a considerable increase in cut-off frequency, above that expected from the physical dimensions of the base region.

## (3) CIRCUIT APPLICATIONS

The combination of very high current gain and greatly reduced transit time makes the avalanche transistor well suited for use in trigger circuits for the generation of fast pulses.

To obtain maximum current gain and minimum transit time the collector must be biased to the breakdown voltage $V_A$. Unfortunately, since $V_A$ differs considerably between transistors, it is not practical to apply the bias directly as a voltage. However, by drawing a defined current from the collector, for example by means of a large resistance connected to a highly negative supply potential, the collector current can be safely limited to a suitable value, and the collector will automatically take up the potential $V_A$.

If the emitter is biased off, the multiplication occurring under these conditions is given by the ratio $I_c/i_{co}$, where $I_c$ is the defined collector current and $i_{co}$ is the collector leakage current measured under normal conditions, i.e. at a low collector voltage. To obtain a high multiplication it is obviously desirable that the collector current should be made as large as possible, but a limit is set by the allowable power dissipation in the transistor. The product $I_cV_A$ should therefore not be allowed to exceed, say, 50 mW for low-power transistors.

### (3.1) The Basic Trigger Circuit

A simple trigger circuit is shown in Fig. 2(*a*). The collector is biased to $V_A$ with a constant current supply $I$, and the emitter

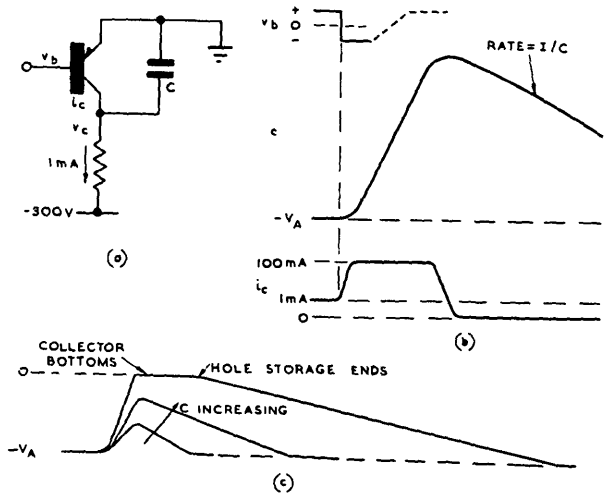



Fig. 2.—Basic trigger circuit.
(*a*) Simple circuit.
(*b*) Waveforms.
(*c*) Effect of C on collector voltage waveform.

is normally held non-conducting by a positive bias applied to the base.

#### (3.1.1) Triggering Action.

A negative input pulse applied to the base causes holes to be injected from the emitter into the base layer, which, on entering the collector depletion layer, are multiplied by a large factor. The resulting collector current is fed back regeneratively to the

emitter by the capacitor C, and a rapid increase of current occurs around the feedback path. The circulating current is prevented from increasing indefinitely by the rise in collector potential away from $V_A$ as C becomes charged. The multiplication factor falls rapidly as the collector voltage decreases from $V_A$, the loop gain is reduced and the rate of rise of current is curtailed. In addition, owing to the change in collector voltage, a progressive decrease occurs of depletion layer width, resulting in an increase in the transit time of holes across the base region, which also reduces the rate of rise of current.

### (3.1.2) The Collector Waveform.

As a result of these effects the current waveform, Fig. 2(*b*), shows a rapid initial rise, and then tends to flatten off to a steady value as the collector voltage moves away from $V_A$. This means that the collector voltage will rise in an approximately linear manner. The rise of collector voltage continues until eventually the multiplication becomes so low that the gain around the regenerative loop is less than unity.

It might be expected that this condition would define the termination of the rise of collector voltage. However, in practice the collector waveform may show a continued rise past this point, which is accounted for by the collection of holes accumulated in the base region during the earlier part of the rise.

### (3.1.3) Hole Storage Effects.

Owing to the large multiplication factor which exists during the first part of the rise of collector voltage, only a small fraction of the charge fed back from collector to emitter via C is actually used to maintain the collector current. The excess charge, which is necessary to maintain the circulating current by multiplication, is stored in the form of holes within the base region, with very little loss due to recombination. However, when the collector voltage has risen sufficiently to destroy the multiplication effect, there is insufficient loop gain to generate further excess charge, and the stored charge within the base is now used up in supplying the losses in the circuit, the circulating current being maintained near its previous level in this way. The termination of the rise of collector voltage occurs when all the stored charge has been used up, and the collector current then falls to $i_{co}$. If the amount of stored charge is sufficiently large, the collector potential may rise temporarily into the bottoming region.

### (3.1.4) Influence of Feedback Capacitor on Collector Waveform Amplitude.

The voltage at which the collector potential ceases to rise depends upon the initial loop gain of the circuit, since this determines the amount of excess charge which is stored during the first part of the rise. Now, in the circuit of Fig. 2 only a fraction of the holes which emerge after multiplication in the collector region go to make up the current circulating through C. A proportion of the multiplied charge is diverted into the depletion layer capacitance $C_c$, and so only a fraction, $C/(C + C_c)$, of the multiplied charge is fed back to the emitter. An effective multiplication factor, $M_{eff} = MC/(C + C_c)$, can be used to denote the charge gain around the loop. The loop gain is therefore a function of the ratio of $C$ to $C_c$, and as $C$ is increased, thus increasing the gain, the amplitude of the collector waveform also increases, as shown in Fig. 2(*c*). Eventually, a value of $C$ may be arrived at which enables the collector to rise from $-V_A$ up to the bottoming potential. The excess holes, which are still stored in the base and have not been used up during the collector rise, then serve to hold the transistor in the bottomed condition for some time. This condition is similar to that of a transistor which is operating in the normal mode and has been heavily bottomed.

### (3.1.5) Influence of Feedback Capacitor on the Rate of Rise of Collector Voltage.

It has already been mentioned in Section 3.1.1 that $M$ falls very rapidly as the collector voltages decreases from its initial value of $-V_A$.

Fig. 3(*a*) shows how $M$ varies with collector voltage. For

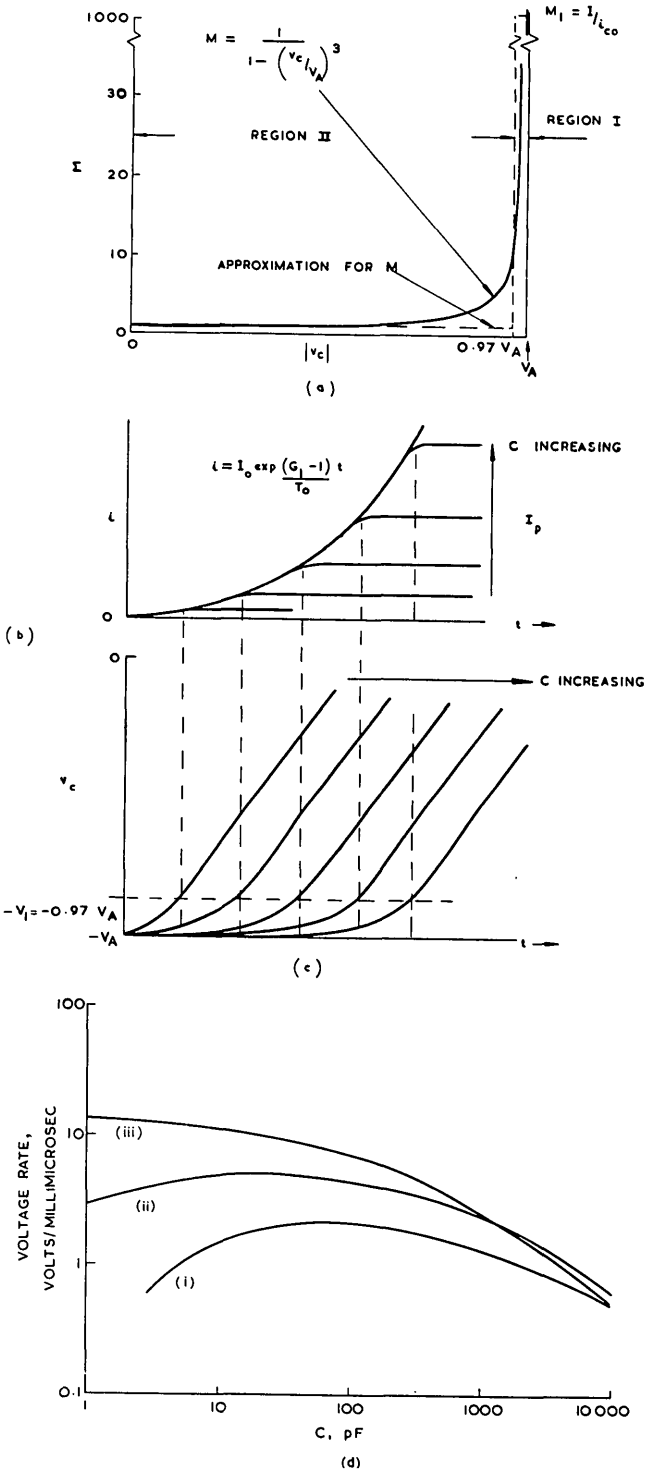



Fig. 3.—Effect of $C$ on rate of rise of $v_c$.

(*a*) Graph of $M = \frac{1}{1 - (v_c/V_A)^3}$
(*b*) Current waveforms.
(*c*) Collector voltage waveforms.
(*d*) Rate of rise of $v_c$.

values of $|v_c/V_A|$ greater than 0·97, $M$ is greater than 10, but below this value of $|v_c/V_A|$, $M$ rapidly approximates to unity. Thus, the operating region of the transistor may be divided into two sections. In the first, where $|v_c| > 0{\cdot}97V_A$, the multiplication factor and, therefore, the loop gain of the regenerative circuit are very large. Whilst the collector voltage remains greater than $0{\cdot}97V_A$, therefore, the current waveform in the circuit will increase rapidly owing to the high loop gain. In the second region, however, where $|v_c| < 0{\cdot}97V_A$, the multiplication factor, and hence the loop gain, is only slightly greater than unity. In this region the current waveform levels off as there is not sufficient loop gain to give rise to a further increase in the circulating current. The collector voltage waveform then assumes a constant rate of rise as the almost constant circulating current is integrated in C. It can be shown that this rate of rise is sensibly independent of $C$ except when this is very small.

For this purpose it will be assumed that for $|v_c| > 0{\cdot}97V_A$ $(=V_x)$, $M$ is large and constant at a value $M_1$. Below the critical voltage $V_x$, $M$ is assumed to have a value such that the loop gain $M\alpha$ is exactly unity. This approximation is indicated by the dotted line in Fig. 3(*a*). ($C$ is assumed to be much greater than $C_c$ so that $M_{eff} \simeq M$.)

For this calculation, the transistor is assumed to have a constant dispersive transit time $T_0$, and a loop gain $G = M\alpha$. During the regenerative period following triggering, the current waveform will therefore have the form

$$i = I_0 \exp \frac{[(G-1)t]}{T_0} \quad . \quad . \quad . \quad . \quad . \quad (1)$$

where $I_0$ is the initial triggering current. The corresponding voltage waveform then has the form

$$v_c = -V_A + v \quad . \quad . \quad . \quad . \quad . \quad (2)$$

where $v = \frac{1}{C}\int i\,dt$,

and may be rewritten as

$$v_c = -V_A + \frac{I_0T_0}{C(G-1)} \exp \frac{(G-1)t}{T_0} \quad . \quad . \quad (3)$$

In the first region, where $G = G_1 \gg 1$, the current and voltage waveforms will follow an exponential shape as shown in Figs. 3(*b*) and (*c*).

The curves are drawn for various values of $C$. The current waveform is the same in all cases, but since $v_c$ contains a variable term inversely proportional to $C$, the voltage waveform will appear to move to the right as $C$ is increased, although the time-constant $T_0/(G_1 - 1)$ in the exponential term remains constant.

In the second region of operation, where $|v_c| < V_x$, the loop gain $G = G_2$ is assumed to be unity and the circulating current is therefore maintained constant at the level at which it stood at the instant of transition from region I to region II. The boundary condition in each case is given by $|v_c| = V_x$. Since the circulating current has a constant value in this region, the voltage rise will now become linear, and the rate of rise of collector voltage is given by

$$(dv_c/dt)_2 = I_2/C \quad . \quad . \quad . \quad . \quad . \quad . \quad (4)$$

where $I_2$ is the steady circulating current.

It will now be shown that $I_2$ is proportional to $C$, and that the rate of rise of voltage $dv_c/dt$ is constant and independent of $C$. $I_2$ may be calculated by finding the value of $i$ when $|v_c|$ becomes $V_x$.

In region I,

$$i = I_0 \exp \frac{(G_1-1)t}{T_0} \text{ and } v = \frac{I_0T_0}{C(G_1-1)} \exp \frac{(G_1-1)t}{T_0} \quad . \quad (5)$$

Hence,
$$i = \frac{C(G_1-1)}{T_0}v \quad . \quad . \quad . \quad . \quad . \quad (6)$$

Thus, when $|v_c|$ has a value $V_x(= 0{\cdot}97V_A)$, $i$ has reached a level

$$I_x = \frac{C(G_1-1)}{T_0}(V_A - V_x) \quad . \quad . \quad . \quad . \quad (7)$$

since $v$ is then $V_A - V_x$.

Now $I_2$ is equal to $I_x$ (the value at the boundary) and thus $I_2$ is directly proportional to $C$ only, assuming the other factors to remain constant.

The voltage rate of rise, $dv_c/dt$, in region II is $I_2/C$, which may be rewritten

$$(dv_c/dt)_2 = \frac{G_1 - 1}{T_0}(V_A - V_x) \quad . \quad . \quad . \quad (8)$$

This is independent of $C$, and so all the voltage waveforms of Fig. 3(*c*) will be parallel to each other at collector voltages above $-V_x$. Fig. 3(*b*) has been drawn to show the levelling off of current at various values of $I_2$ which occurs with different values of $C$.

The above analysis assumes that in all cases $C$ is large compared with $C_c$ so that $M_{eff} = M$. At small values of $C$ the rate of rise of voltage above $-V_x$ becomes dependent upon $C$. Taking the result derived for $dv_c/dt$, eqn. (8), and now including $M_{eff}$ in the expression for loop gain, we obtain

$$\left(\frac{dv_c}{dt}\right)_2 = \frac{(G_1-1)(V_A - V_x)}{T_0}$$

$$= \frac{[\alpha M_1 C/(C + C_c) - 1](V_A - V_x)}{T_0} \quad . \quad . \quad . \quad (9)$$

When the value of $C$ is comparable with that of $C_c$, $M_{eff}$ is considerably reduced, and $(dv_c/dt)_2$ thus becomes much smaller than when large values of $C$ are used. The result of reducing $C$ to a very small value is therefore to decrease the rate of rise of voltage, whilst at large values of $C$ the rate of rise of voltage should remain constant.

The effect of $C$ upon the actual rates of rise of three typical avalanche transistors is shown in Fig. 3(*d*). Curve (i) represents a transistor with relatively slow response, and shows clearly the increase in speed obtainable by increasing $C$ from very low values. Curve (ii) is for a rather faster transistor, and shows the same type of variation, whilst curve (iii) is for a very fast transistor, where the speed is so high that even the stray capacitance enables the maximum rate of rise to be attained. For all three types, however, there is a falling off in the rate of rise at high values of $C$, which is attributed to the limiting effect of lead inductances when the rate of rise of circulating current is very high. Some estimate of this effect may be obtained by considering curves (ii) and (iii) when $C = 1\,000$ pF. The voltage rate is then $2{\cdot}5 \times 10^9$ volts/sec, and the peak current is therefore 2·5 amp. The current builds up to this peak value in a few millimicroseconds, so that the rate of rise of current is of the order of $10^9$ amp/s. A lead inductance of only $10^{-8}$ H in the transistor is therefore sufficient to cause a drop of 10 volts, which subtracts from the voltage apparently being applied to the transistor, and decreases the collector voltage sufficiently to cause a large reduction in $M$. The rise in circulating current thus becomes prematurely curtailed, and the rate of rise of voltage is lower than that otherwise predicted for high values of $C$. This trend is shown clearly for all three types of transistor.

### (3.2) The Generation of Short-Duration Pulses

As the collector voltage rise is approximately linear, the rise time can be estimated from Fig. 3(*d*) by dividing the rate of

rise into the total voltage excursion. Thus, for $C = 1\,000$ pF, assuming $V_A$ to be 50 volts, the transistor of curve (iii) in Fig. 3(*d*) has a rise time of $50/2{\cdot}5 = 20$ millimicrosec. For small values of capacitance, the collector does not rise sufficiently to bottom, and the waveform amplitude is not accurately known. However, for fast transistors of type (iii), even at very small values of $C$ the excursion is approximately $\frac{1}{2}V_A$, increasing, of course, as the value of $C$ is increased. Thus, the rise time with $C = 3$ pF is of the order of $25/12{\cdot}5 = 2$ millimicrosec, the rate of rise being 12·5 volts/millimicrosec. As $C$ is increased from this value the rate of rise decreases gradually, whilst the waveform amplitude increases, so that the rise time also increases. The shortest rise time is thus obtained with very small values of $C$.

By suitably differentiating the resulting collector waveform, very narrow pulses of a few volts amplitude may be obtained, with a width corresponding to the above rise time.

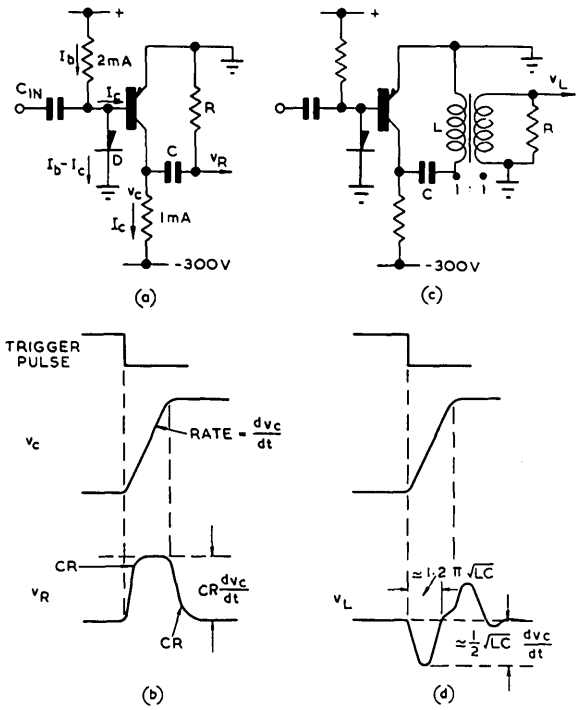



**Fig. 4.**—Practical circuit.
(*a*) Circuit.
(*b*) Waveforms.
(*c*) Use of inverting transformer.
(*d*) Waveforms.

(3.2.1) **Practical Circuit.**

A simple method of obtaining the required output waveform is to insert a low resistance, $R$, in series with $C$ [Fig. 4(*a*)]. In this circuit, a hold-off bias is supplied to the base by the forward conducting potential of the diode D. When the emitter is thus biased off, the whole of the collector current $I_c$ flows in the base. $I_b$ must therefore be made greater than $I_c$ in order to supply the latter and also to provide a difference current which flows in D to provide the bias. Triggering is achieved by means of a negative pulse applied to the base, which lowers the base potential below that of the emitter and therefore injects holes at the emitter to initiate the regenerative process.

The output waveform is developed across R and the time-constant $CR$ is made much less than the desired pulse width in order to obtain full differentiation. The amplitude of the output pulse is given by $CR$ times the voltage rate of rise at the collector.

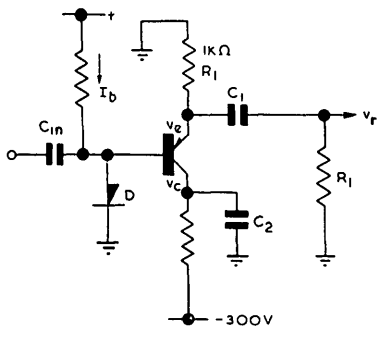
The values of $C$ may be chosen arbitrarily to some extent, but very small values of $C$ limit the current available in the output pulse, and larger values slow the rate of rise of the collector voltage, and therefore give wider output pulses. Typical values to obtain the waveform of Fig. 4(*b*) are $C = 3$ pF, $R = 100$ ohms, giving an output pulse of over 3 volts amplitude and 2 millimicrosec width.

(3.2.2) **Output Pulse Inversion.**

An inverted output pulse may be obtained by interposing a transformer between C and R [Fig. 4(*c*)]. The use of a tube of nickel-zinc ferrite as a transformer core has proved to be very convenient, since it may be slipped over the capacitor lead wire and provides good coupling to the secondary wire with a minimum of stray capacitance. In addition, the primary inductance may be chosen (by selecting the correct grade of ferrite), to resonate with $C$. The load, $R$, then provides suitable damping so that further waveform shaping occurs, resulting in narrower pulses, but having reduced amplitude if the values of $C$ and $R$ remain unchanged. Thus, with $C = 3$ pF, and $R = 100$ ohms as before, making $L = 0{\cdot}025\ \mu$H yields a pulse of 1 millimicrosec width with an amplitude of about 1·5 volts [Fig. 4(*d*)].

(3.2.3) **Circuit Recovery Time.**

The recovery time of the circuit is governed by the rate of recharge of collector circuit capacitance to $V_A$ from the voltage at which the avalanche rise terminates. Assuming, as before, that the collector voltage rises through 25 volts, the collector-base capacitance $C_c$ and the circuit capacitance $C$ must be recharged through this voltage by the current $I_c$, which in this case is 1 mA. A typical mean value of $C_c$ in the voltage range 25–50 volts is 10 pF, and so with $C = 3$ pF, the recovery time is



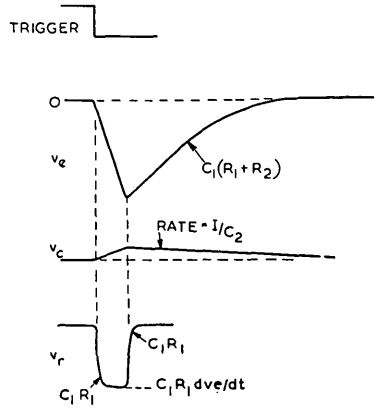




**Fig. 5.**—Negative pulse generator.

$\frac{(10+3)\times 25\times 10^{-12}}{1\times 10^{-3}} = 325$ millimicrosec. In this instance, therefore, the maximum repetition frequency of the circuit is limited to 3 Mc/s. This maximum rate is greatly reduced in circuits where the collector is allowed to bottom, as the hole storage time is then considerable.

### (3.3) Alternative Fast-Pulse Generator

As an alternative to the use of transformers to obtain negative-going pulses, a common-collector configuration may be adopted. A typical circuit is shown in Fig. 5. The emitter is returned to earth potential through a comparatively high resistance (1 kilohm) and the base is biased as before with a diode D and a current supply $I_b$. The collector circuit capacitance $C_2$ is now made very large, so that the collector is effectively earthed to pulse currents. When a negative pulse is applied to the base, the circuit triggers and attempts to clamp emitter and collector together. Since the collector potential is held almost immovable by $C_2$ the output waveform appears at the emitter, in the form of a fast negative-going edge which is differentiated by $C_1$ and $R_1$ to produce the required output waveform.

During the triggering process the collector potential will have changed slightly, the charge passing through $C_1$ being subtracted from the total charge on $C_2$. The base potential will also have followed the emitter in a negative direction. The recovery time of the circuit is therefore the time taken for the current supply $I_c$ to replace the lost charge on $C_2$, and to recharge the collector-base capacitance. In addition, the trigger input capacitor $C_{in}$ requires recharging, so that this circuit takes longer to recover than the corresponding common-emitter circuit. However, by adopting a different method of triggering, for instance a transformer winding in series with D, the effect of $C_{in}$ may be eliminated, in which case the recovery time is similar to that of the common-emitter circuit.

### (3.4) Pulse Shaping by means of Diode Capacitance

The methods so far described for deriving short-duration pulses from the collector waveform of an avalanche transistor have the following limitations:

(*a*) Differentiating the avalanche rise yields pulses whose width is determined by a rise time of the original waveform.
(*b*) Obtaining pulses of shorter duration by exciting a damped resonant circuit can only be done at the cost of a reduction in pulse amplitude.

To obtain pulses of duration shorter than the avalanche rise time without using method (*b*) demands the use of a non-linear element to enable part of the waveform, and therefore part of the total rise interval, to be selected. Suitable diodes for this application cannot readily be obtained, as hole storage and conductivity modulation effects are extremely serious in even the best diodes with the fast waveforms under discussion.

A suitable non-linear element, however, is the capacitance which appears across a reverse-biased junction diode. For alloy junctions, this capacitance varies approximately as the inverse

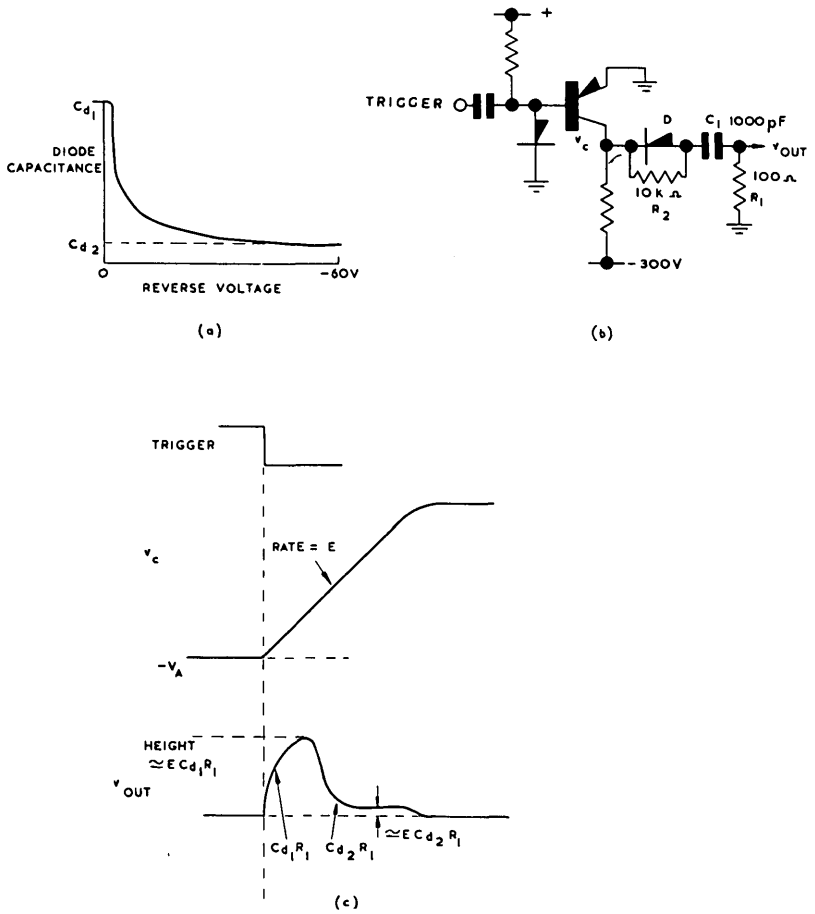



Fig. 6.—Pulse shaping.
(*a*) Variation of diode capacitance with voltage.
(*b*) Use as pulse shaping element.
(*c*) Waveforms.

square root of the applied voltage. Thus, at a low applied voltage a large capacitance is measured which decreases to a very small value as the voltage increases, as shown in Fig. 6(*a*).

This non-linear property is applied to the generation of narrow pulses in the circuit of Fig. 6(*b*), where the fixed capacitor of the differentiating network of Fig. 4(*a*) is replaced by the capacitance of a diode, D. The blocking capacitor C is charged up to $-V_A$ through $R_2$ whilst the circuit is quiescent, so that the diode is in the zero-bias condition and exhibits maximum capacitance. However, when the circuit is triggered, the collector voltage rises towards zero from $-V_A$ and applies a reverse bias to the diode, so that its capacitance becomes small. The collector waveform is therefore operated upon by a differentiating circuit whose time-constant is initially large but rapidly falls to a smaller value. As a result, an output pulse appears only during the first fraction of the total rise interval, practically no output voltage appearing when the differentiating network is in its small-time-constant state. This is illustrated by the waveforms of Fig. 6(*c*).

### (3.5) Application to Fast-Rise Blocking Oscillators

The advantages of fast sensitive triggering associated with the avalanche mode of operation may be extended to blocking oscillator circuits, enabling long (microsecond) pulses of well-defined duration to be generated with a rise time of a few millimicroseconds.

A typical circuit is shown in Fig. 7(*a*), where, in the quiescent condition, the transistor is biased to the avalanche region by means of a collector bias current as previously described. The base is supplied with a hold-off bias developed across $D_1$. If a negative pulse is applied to the base, triggering occurs owing to the avalanche effect, the necessary feedback from collector to emitter being supplied by $C_1$. As a result, the collector voltage rises rapidly from $-V_A$ towards bottoming. As soon as the collector voltage has risen to $-12$ volts, diode $D_2$ starts to conduct, and after that a voltage is developed across the primary winding of the transformer as the collector continues to rise. Positive feedback is now provided by the transformer secondary winding in the emitter circuit, and as a result, the transistor is held in the bottomed condition for a time determined by the transformer and circuit constants. The circuit in fact acts as a blocking oscillator once the avalanche rise has been completed. Diode $D_3$ is included to limit the excursion of the base potential during the interval when the blocking oscillator returns to the quiescent condition.

In the basic circuit described, there may be a delay between the application of a trigger pulse to the base and the appearance of a voltage pulse across the transformer windings, corresponding to the time taken for the collector to rise from $-V_A$ to $-12$ volts. There may also be a large voltage drop across $D_2$ when it begins to conduct (conductivity modulation) which prevents the imme-

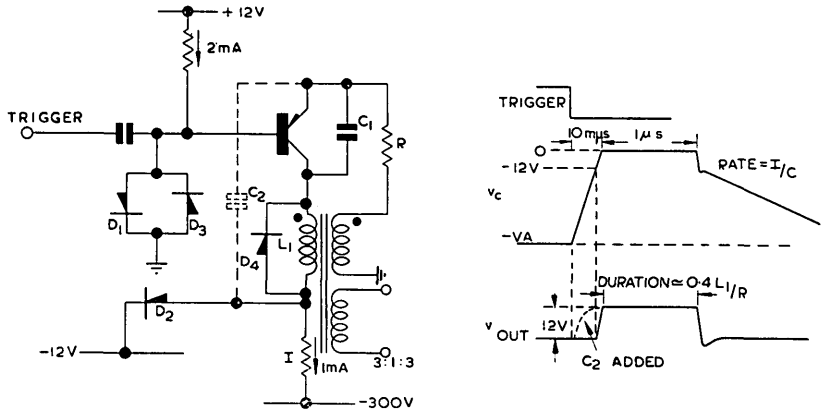



Fig. 7.—Wide-pulse generator.

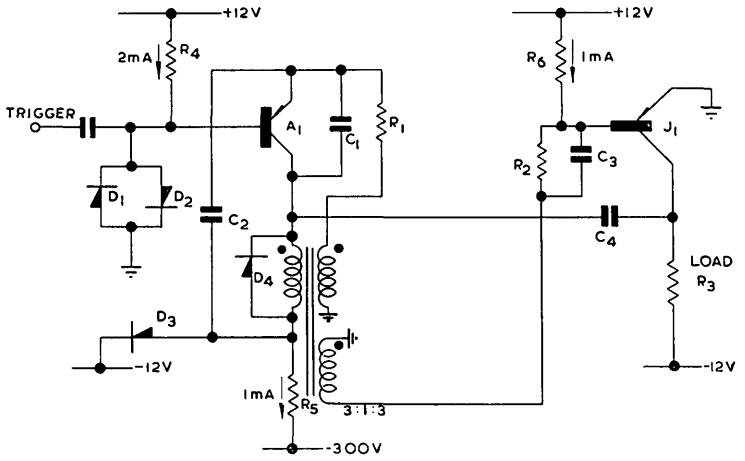



Fig. 8.—Addition of output stage to Fig. 7.

| | | | | | |
|---|---|---|---|---|---|
| $R_1$ | 100Ω | $C_1$ | 47pF | $D_1$ | CV2290 |
| $R_2$ | 1kΩ | $C_2$ | 100pF | $D_2$ | CV2290 |
| $R_3$ | 100Ω | $C_3$ | 1000pF | $D_3$ | OA5 |
| $R_4$ | 5·6kΩ | $C_4$ | 100pF | $D_4$ | CV448 |
| $R_5$ | 270kΩ | | | | |
| $R_6$ | 10kΩ | | | | |

diate application of the full 12 volts to the transformer primary winding. However, these defects can be overcome by the addition of another capacitor, $C_2$, shown dotted.

$C_2$ reduces the rate of rise of potential of the lower end of $L_1$ compared with that of the collector end during the initial avalanche rise. As a result a voltage difference is developed across $L_1$ as soon as triggering occurs, which appears at the emitter winding to provide positive feedback. The delay incurred in waiting for the collector to rise to $-12$ volts (when $D_1$ begins to conduct) is therefore eliminated, and the steady 'on' state, with the circuit acting in the normal blocking-oscillator mode, is achieved sooner. The circuit values may be chosen so that the contribution to the output pulse due to the addition of $C_2$ makes up for the lags caused by the leakage inductance of the transformer and the voltage drop in $D_2$, giving an output pulse with a fast rise and a flat top.

### (3.6) Fast-Rise Pulse Generator

Occasionally a circuit is required which supplies a pulse of defined length into a load of varying impedance. In such a case a blocking oscillator is unsuitable, since a load connected directly across the transformer affects the timing. A transistor buffer stage may be used to overcome this disadvantage (Fig. 8). Owing to the relatively poor frequency response of the buffer transistor, which is operated in the normal mode, the fast initial edge cannot be transmitted by this stage, although a certain amount of speed-up is caused by $C_3$ in the base circuit. The buffer stage is therefore by-passed by $C_4$, which transmits the initial rise of potential of the collector of $A_1$ directly to the load, whilst $J_1$ operates rather more slowly to maintain the top of the pulse. Here again the circuit values may be chosen to obtain a fast-rise pulse with a flat top.

## (4) GENERATION OF ACCURATELY DELAYED PULSES

In many applications it is required to produce pulses which are related to a previous event by a known delay. This can usually be achieved by applying a ramp function, initiated by the first event, to the trigger terminal of the pulse generator

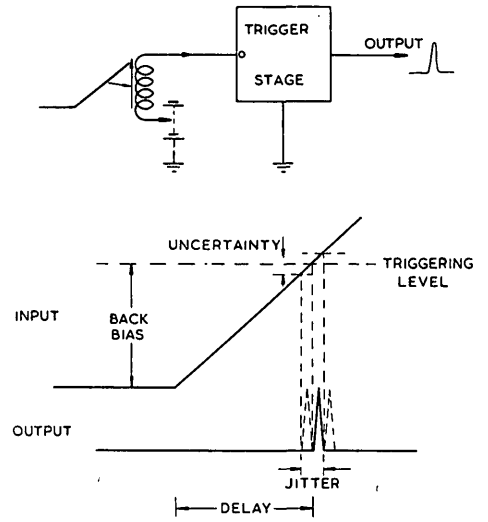



Fig. 9.—Method of generating delayed pulse.

(Fig. 9), the delay being determined by the amount of back-bias which has been applied to the triggering waveform.

### (4.1) Threshold Stability

The accuracy of the delay depends upon the stability of the triggering threshold, and will be affected by drift or random variations of threshold level.

#### (4.1.1) D.C. Threshold Stability.

The measurements plotted in Fig. 10, showing the variation in d.c. threshold level against temperature for a typical fast-rise avalanche transistor, indicate that the drift of threshold level with temperature is linear and relatively small, having a rate of

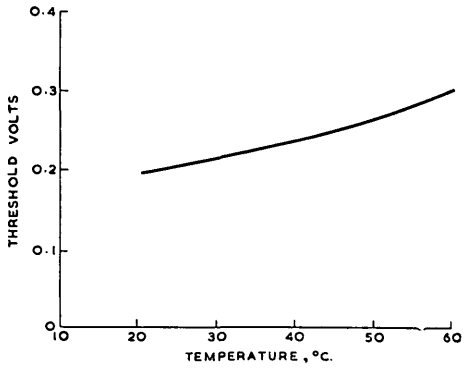



Fig. 10.—Drift of threshold voltage with temperature.

about 2·5 mV per deg C. This figure corresponds closely to the theoretical value calculated for a germanium $p$–$n$ junction, and suggests that the drift may be largely eliminated by compensating with a junction diode. However, when input voltage swings in the region of 5 volts are used, compensation is probably unnecessary, as the drift is then only about 0·05% per deg C.

#### (4.1.2) Threshold Noise.

Apart from a slow drift due to temperature, a slight random variation in threshold level is experienced with many avalanche transistors which originates in the noise generated at the collector junction.

A collector junction biased to the breakdown region exhibits small random variations of breakdown voltage as different sections of the junction break down in turn, and conduct the 1 mA bias current for a short while.[9] Owing to local irregularities, various sections will have different breakdown voltages, and the resulting variations in avalanche voltage appear as noise at the collector terminal. The peak-to-peak amplitude of this noise is generally of the order of 10 mV.

The variations in avalanche voltage cause the boundary of the collector depletion layer to fluctuate in position, giving rise to a modulation of the active base width. In a fast avalanche transistor, where the base width has become very small, such a variation can form an appreciable proportion of the whole width, so that, as the cross-section of the base fluctuates, the base resistance may vary appreciably. The voltage drop in the base due to the passage of the 1 mA bias current to the collector therefore exhibits a noise component, which gives rise to a random variation in the threshold level of triggering as measured at the external connections of the emitter-base diode. The noise voltage appearing across the base resistance may be examined by means of a high-impedance probe connected to the emitter terminal, which is otherwise left floating. Coupling to the internal base connection is by means of the emitter depletion-layer capacitance. Peak-to-peak noise readings of the order of 0·5 mV are obtained at the emitter by this method.

From this figure, the amount of jitter which is likely to be present on a delayed pulse can now be calculated. Thus, if the input ramp has a slope of 1 volt/microsec = $10^6$ volts/sec, the jitter caused by 0·5 mV of noise on the threshold level is $0{\cdot}5 \times 10^{-3}$ volt/($10^6$ volts/sec) = 0·5 millimicrosec.

### (4.2) Typical Circuit

A typical delay circuit is shown in Fig. 11. In this case the polarities of the waveforms shown in Fig. 9 are inverted. The base is normally biased off by an amount $+V$, which is applied through the transformer secondary winding and diode D.

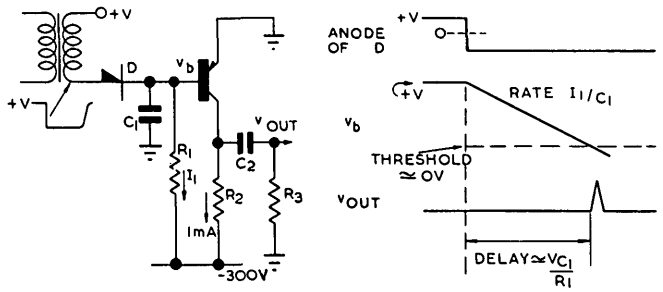



Fig. 11.—Delayed-pulse generator.

A negative ramp at the base is initiated by a fast negative-going waveform applied to the anode of D, which renders the latter non-conducting and allows the base potential to fall at a rate determined by the charging current $I_1$ flowing in capacitor $C_1$. Triggering occurs when the base potential has fallen through approximately $V$ volts to its threshold level. The delay obtained is thus approximately $VC_1/I_1$. ($I_1$ is assumed to be constant since $V \ll 300$ volts.) The output pulse appears across $R_3$ in series with $C_2$ in the usual manner. Alternatively, a transformer may be employed, as in Section 3.2.2.

### (5) SELECTION OF AVALANCHE TRANSISTORS

At present no specific avalanche transistors are commercially available, though the design features appear to be well understood. Suitable units are therefore selected from normal medium-frequency transistor production batches. So far, it has not been found possible to predict accurately the characteristics of avalanche transistors other than by a dynamic test. This involves testing the transistor in the basic circuit of Fig. 2 and requires an oscillograph system of sufficient bandwidth to resolve rise times of 1 or 2 millimicrosec. In the absence of such an oscillograph, it is possible, with certain cathode-ray tubes which have very short leads to the Y-deflection plates, to observe the collector waveform by making a direct connection to the plates, no amplifier being necessary, since a relatively large waveform is being observed. In such cases, the bandwidth of the viewing system is adequate.

Alternatively, the differentiating circuit of Fig. 4(*a*) may be used with the addition of a peak-reading meter system which indicates the height of the differential pulse. In this case the highest reading will correspond to the highest rate of rise of collector waveform. Transistors which exhibit the punch-through effect will tend to oscillate in the test circuit, but can be eliminated by rejecting transistors which give a reading in the absence of an input trigger pulse. Typical selection figures are given in Table 1. It has been noted that some avalanche transistors are faster when the emitter and collector connections have been reversed. The figures quoted include transistors exhibiting this effect.

**Table 1**

| Type | Total | Rise times, millimicroseconds <1·5 | 1·5–3 | 3–10 | >10 | Unsuitable |
|---|---|---|---|---|---|---|
| XA101 .. .. | 25 | 2 | 0 | 2 | 19 | 2 |
| V6/R8 .. .. | 12 | 1 | 1 | 1 | 4 | 5 |
| 2N267 .. .. | 5 | 0 | 0 | 2 | 0 | 3 |
| 2N247 .. .. | 7 | 0 | 1 | 1 | 2 | 3 |
| XA102 .. .. | 100 | 8 | 15 | 25 | 0 | 52 |
| OC44 received between May and September, 1958 | 648 | 30 | 37 | 112 | 37 | 484 |
| OC44 October, 1958 .. | 200 | 7 | 3 | 12 | 14 | 164 |
| OC44 November, 1958 | 900 | 10 | 15 | 63 | 86 | 726 |

### (6) CONCLUSIONS

Trigger circuits have been described which are capable of generating millimicrosecond pulses and have a threshold stable to less than 0·1 volt. An attractive feature of these circuits is their simplicity and small size.

Although selection of transistors is necessary to obtain the highest speeds, it is felt that the yields are sufficient to justify this practice in commercial equipment. Some of the so-called 'four-layer diodes' which are being made today rely partially on the avalanche effect for their operation, and it is likely that the diffusion techniques used in these 'diodes' could be directed to making reproducible avalanche transistors.

The intrinsic switching time of the avalanche effect is at least an order of magnitude shorter than the times reported in the paper, and it is felt that devices realizing shorter rise times would find useful applications.

### (7) ACKNOWLEDGMENTS

The authors would like to thank Mr. E. H. Cooke-Yarborough and Dr. C. J. N. Candy for many helpful discussions, and also Mr. A. J. Cole, who carried out several of the measurements, including the large number of selection measurements reported in Table 1.

A very stimulating meeting with Dr. W. Shockley of Beckman Instruments, Inc., is also acknowledged with gratitude.

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