Discrete-Time Parametric Amplification Based on a Three-Terminal MOS Varactor: Analysis and Experimental Results

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***Abstract*—This paper discusses discrete-time parametric amplification based on large-signal operation of a three-terminal MOS varactor. The principle of operation is described in detail and analytical estimates of performance are derived. Detailed measurements are reported for a prototype implemented in standard digital CMOS technology. It is demonstrated that the technique can be used to provide micropower, low-gain, low-noise, large-signal amplification.**

***Index Terms*—Discrete-time amplification, MOS varactor, parametric amplifier.**

I. Introduction

A PARAMETRIC amplifier is a circuit in which amplification is achieved by the use of variable (time-dependent) parameters or circuit elements [1]. The use of these amplifiers in continuous-time applications, including frequency division [2], resonant circuit amplification [3], and synchronous detection [1], is well known. The main motivation in using this approach is that the resulting implementations have low noise. The input frequency in the classical approach typically must have a specific relation to the frequencies of one or more controlling signals. One of the frequently used parametric elements is a two-terminal nonlinear capacitor. In a typical application using this capacitor, a large control signal varies the value of the capacitor while a small input signal over the control signal sees a time-varying linear capacitor. Since both signals face the same capacitor characteristic, the amplitude of the input signal is severely limited. One method to accommodate larger inputs is to use a three-terminal capacitor which can separate out the characteristics seen by the input and the controlling signal. However, implementations of parametric amplifiers based on three-terminal capacitors have mostly used either mechanical [3] or optical control.

In this paper, a discrete-time parametric amplifier is described which uses a three-terminal MOS varactor switched between two modes [4], [5]. The use of this varactor enables the input signal as well as the control signal to be electronic. The amplification is performed on sampled-and-held data. Restrictions which classical parametric amplifiers place on input frequency, are relaxed: even signals arbitrarily close to dc can be amplified. The amplifier can be used in applications that involve sampling, including the input stage of an analog-to-digital converter, or a clocked comparator to reduce input referred errors, or a subsampling mixer. It can also be used in switched-capacitor filters incorporating changes in capacitance between charge and dump phases.

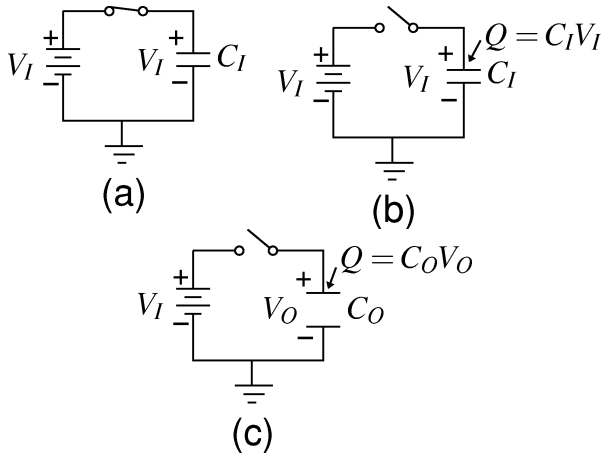

Fig. 1. Discrete-time parametric amplification principle phases shown are: (a) track, (b) hold, and (c) boost.

The basic technique is illustrated with linear parallel-plate capacitors in Fig. 1. A dc input source is assumed for simplicity. In the track phase, shown in Fig. 1(a), an input voltage V_I is being tracked on a capacitor C_I. At the beginning of the hold phase the input switch is opened. The input voltage at the sampling instant V_I is held on the capacitor as shown in Fig. 1(b). The charge on the top plate of the capacitor is $Q = C_I V_I$. With the input switch open, there is no circuit path to the top plate of the capacitor and the charge on it does not change. The third phase, called the boost phase, is shown in Fig. 1(c). In this phase, while the input switch is open, the plates of the parallel-plate capacitor are, assumed to have been moved apart (this is used only to illustrate the principle). This results in a reduced capacitance C_O. The voltage across the capacitance V_O is Q/C_O, where Q is $C_I V_I$. This gives

$$V_O = \left(\frac{C_I}{C_O}\right) V_I. \tag{1}$$

Amplification of a sampled voltage is thus achieved. The boosted value of the capacitor voltage will be considered to be our output.

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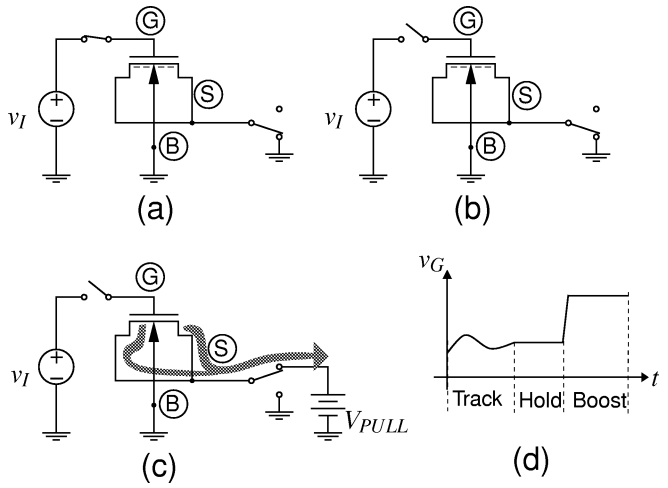

Fig. 2. Discrete-time MOSFET parametric amplifier in: (a) track, (b) hold, (c) boost phases. (d) Shows the gate voltage.

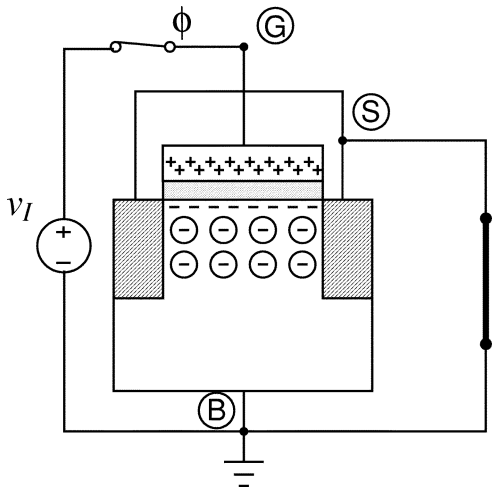

Fig. 3. Track phase. Charges associated with the oxide and with the source–bulk and drain–bulk junctions are not shown for simplicity.

The sampling process does involve the so-called "sampling noise" (or kT/C noise). However, once held data is available, no resistors or active components are used in moving from the hold phase to the boost phase. This implies that there are no sources of noise involved in the amplification process; the amplification *after* sampling is, therefore, ideally noiseless.

II. MOSFET Parametric Amplifier

A. Principle of Operation

A MOSFET-based discrete-time parametric amplifier is shown in Fig. 2. The three-terminal varactor is implemented using the four-terminal MOS transistor by shorting its drain and source together and using them as one terminal called the source (S). The capacitance of interest is between the gate (G) and ground, while the source terminal is the control terminal.

In the track phase shown in Fig. 2(a), the source is grounded and the input is tracked on the gate. The input voltage is assumed to be large enough to produce inversion charges, as is shown schematically in the figure under the gate. At the beginning of the hold phase, the input switch is turned off as shown in Fig. 2(b). The sampled input voltage is now held on the gate. In the boost phase, as shown in Fig. 2(c), the source is switched to a large voltage $V_{\rm PULL}$. This pulls out all the inversion charges from under the gate, and the gate voltage increases, as shown in Fig. 2(d). The reason for this increase is now explained.

The cross section of the nMOS transistor in the track phase [corresponding to Fig. 2(a)] is shown in Fig. 3. The input is being tracked on the gate, while the source is connected to ground. The gate charges are shown as plus symbols on the gate. The inversion charges and depletion charges are represented as minus symbols and minus symbols within circles, respectively.

At the beginning of the hold phase, the input switch is opened. This is shown in Fig. 4. The input voltage at the sampling instant is now held on the gate and the gate charge is fixed. The sampled-and-held voltage is assumed to be large enough to have caused strong inversion; the gate charge Q_G then requires both a depletion charge Q_B and an inversion charge Q_I to compensate for it. The effective oxide interface charge is assumed to be zero for simplicity. From charge neutrality, we have

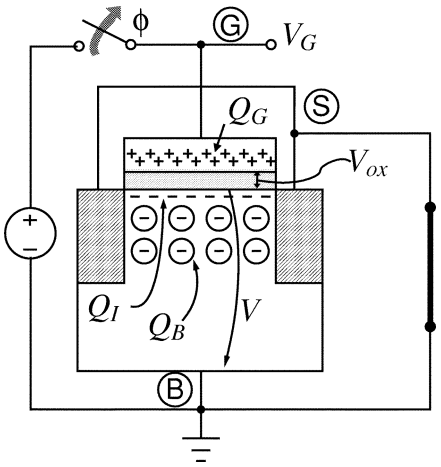

Fig. 4. Hold phase.

$$Q_G = |Q_B| + |Q_I|. \tag{2}$$

The gate voltage V_G is given by (the work function difference is assumed to be zero for simplicity)

$$V_G = V_{\rm ox} + V \tag{3}$$

where $V_{\rm ox}$ is the potential drop across the oxide and V is the surface potential (the potential drop from the oxide–semiconductor interface to the bulk).

The potential drop across the oxide is

$$V_{\rm ox} = \frac{Q_G}{C_{\rm ox}} \tag{4}$$

where $C_{\rm ox}$ is the oxide capacitance. It can be seen that this potential is only a function of the gate charge. The potential drop across the bulk is a monotonically increasing function of $|Q_B|$ (proportional to $|Q_B|^2$, as it turns out [6].) The inversion charge forms a thin sheet of charge right under the gate and is exponentially related to the potential dropped across the bulk.

In the boost phase, shown in Fig. 5, while the input switch is kept off, a large voltage $V_{\rm PULL}$ is connected to the source

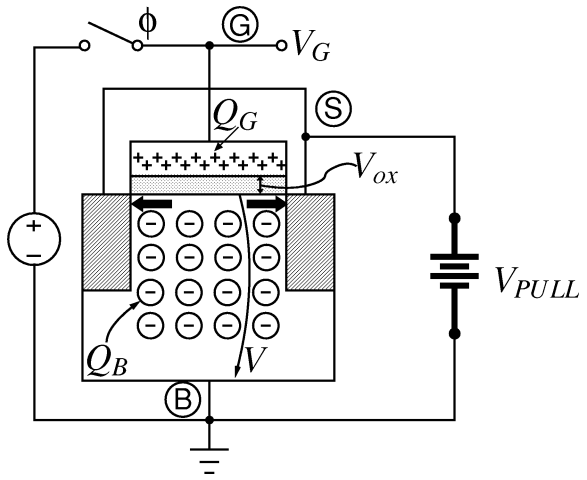

Fig. 5. Boost phase.

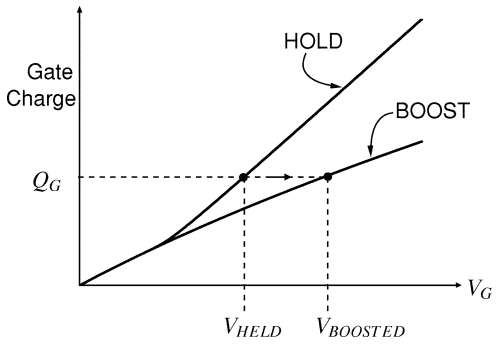

Fig. 6. Gate charge versus gate voltage for hold and boost phases.

terminal. Since the gate is floating, the gate charge remains unchanged. However, the large voltage at the source pulls out all the inversion charge from under the gate and changes Q_I to zero. Now all of the gate charge must be balanced by Q_B, which thus increases in magnitude to satisfy

$$|Q_B| = Q_G. \tag{5}$$

Correspondingly, the potential drop across the depletion region, V, being proportional to $|Q_B|^2$, also increases. On the other hand, the potential drop across the oxide remains unchanged, as seen from (4) and the fact that Q_G has remained the same. We thus see from (3) that the gate voltage increases.

The boosting operation can be illustrated as shown in Fig. 6. The upper curve shows the total gate charge versus gate voltage during the hold phase, in which the inversion layer is allowed to form [6]. The lower curve shows the same quantity during the boost phase, when the inversion layer is removed. Since the gate charge remains constant between the hold and boost phases, the gate voltage is boosted from the value V_{HELD} to the value V_{BOOSTED}. A typical waveform for the switch control, source, and gate voltages is shown in Fig. 7. Bias and signal are indistinguishable for a single sampled voltage, but it is possible to differentiate between them in a differential setup. Small-signal gain is analyzed in a differential circuit next.

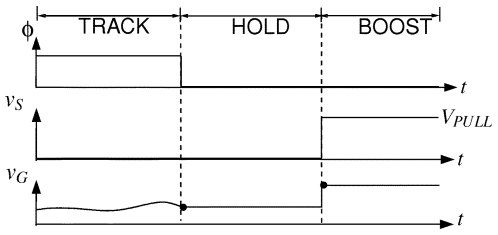

Fig. 7. Typical voltage waveforms.

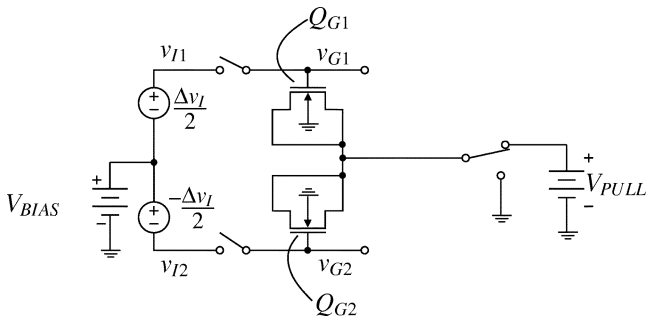

Fig. 8. Differential operation.

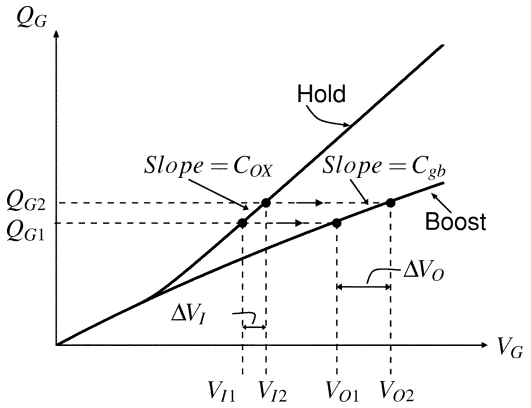

Fig. 9. Gate charge versus gate voltage for hold and boost phases.

B. Differential Operation

Two circuits of the type shown in Fig. 2 can be combined to produce the differential circuit in Fig. 8. The two input voltages v_{I1} and v_{I2} each consist of a common bias component and a differential component as shown. Let the sampled voltages at the gate be V_{I1} and V_{I2}, with their difference denoted by ΔV_I. Repeating the process illustrated in Fig. 6, we obtain the situation shown in Fig. 9. The differential sampled-and-held voltage in the boost phase, ΔV_O, is defined as the output of the circuit. To determine the small-signal gain, $\Delta V_O/\Delta V_I$, note that the slopes of the two characteristics in Fig. 9 are the corresponding small-signal capacitances of the structure in the two phases. In the hold phase, inversion charges are present right under the gate. These form a conducting bottom plate and shield the gate from the depletion charges. The structure resembles a parallel plate capacitor with the distance between the plates equal to the oxide thickness. The capacitance of the structure in the hold phase is, hence, equal to the oxide capacitance C_{ox}. In the boost phase, in the absence of inversion charges, the capacitance of

the structure is the series combination of the oxide capacitance and the depletion capacitance; this combination will be denoted by C_{gb} and is smaller than $C_{\rm ox}$. The changes ΔV_O and ΔV_I can be related through the slopes of the characteristics, as seen from Fig. 9. This produces

$$\Delta V_O = \left(\frac{C_{\rm ox}}{C_{gb}}\right)\Delta V_I \tag{6}$$

which corresponds to (1). The value of C_{gb} can be determined for a given bias using classical MOS transistor models [6]. Typical gain values vary from 5 to 10, depending on the fabrication process. The gain is larger for devices with small body effect (smaller N_A and/or thicker oxide).

The gain derived above is the unloaded gain, i.e., it is based on the assumption that the gate is floating. Parasitic and load capacitances, present at the gate, share the gate charge during boosting and reduce the gain. If a parasitic capacitance C_p is present in both phases, the gain becomes

$$\Delta V_O = \left(\frac{C_{\rm ox}+C_p}{C_{gb}+C_p}\right)\Delta V_I. \tag{7}$$

The gain is insensitive to the exact value of $V_{\rm PULL}$ as long as the latter is large enough to remove the inversion charges. The value of $V_{\rm PULL}$ must be such that, during boosting, the threshold voltage of the device is at least several tenths of a volt higher than the maximum anticipated gate voltage, so that the inversion layer can be completely removed.

There are two main advantages of differential operation. First, the boosted bias voltage only appears as a common-mode voltage and can be rejected easily. Second, the even-order distortion, in particular the second-order distortion which is the dominant one in a single-ended amplifier, is ideally eliminated in differential operation.

C. Noise Considerations

The discrete-time parametric amplifier uses a sampled input. The sampling process introduces kT/C noise due to the sampling of the noise produced by the resistance of the input switch [7]. The parametric amplification process, in principle, does not add any noise to the sampled data. The noise sampled at the input is amplified at the output along with the signal, without degrading the signal-to-noise ratio. However, in a practical circuit, the measured output noise will be larger than this due to sources of noise in the circuit. These sources of noise include the substrate resistance that appears in series with the depletion capacitance during the boost phase, noise in the power supply and noise due to any following buffers as shown in Fig. 10. The substrate resistance noise can be made low by ensuring that all points in the substrate below the gate have a low-resistance path to ground. This can be achieved by surrounding the device with a large number of substrate contacts. The noise in the $V_{\rm PULL}$ supply does not affect the main structure, as long as $V_{\rm PULL}$ is large enough to completely remove the device's channel during boosting (see above). This is because with the channel removed, $V_{\rm PULL}$ is cut off from the rest of the structure. Some influence of the noise in $V_{\rm PULL}$, though, can still find its way to the gate through the gate–drain and gate–source overlap capacitances.

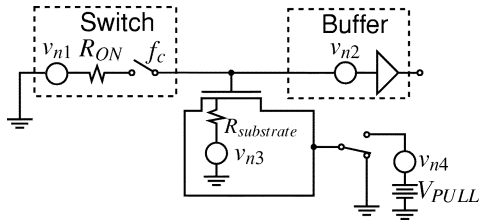

Fig. 10. Noise sources in a practical parametric amplifier.

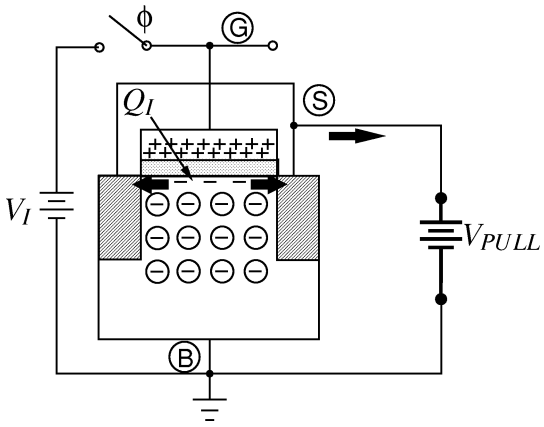

Fig. 11. Considerations in power dissipation calculations.

To quantify the noise performance, an added noise factor (akin to the classical noise factor) is defined for this structure as the ratio between the measured output noise and the output noise expected due to only the theoretical input sampling noise over the same bandwidth.

The fraction of kT/C noise that appears at the output depends on the duty cycle. For a 50% duty cycle for the boost phase, the total integrated sampled noise before amplification in the bandwidth 0 to $f_c/2$ (f_c is the sampling frequency) can be calculated to be $0.117\,(kT/C)$.

The added noise factor over this bandwidth can thus be expressed as

$$\text{Added Noise Factor} = \frac{\text{Total Output Noise (Integrated over}\,f_c/2)}{(0.117\,(kT/C)) \times (\text{Voltage Gain})^2 \times 2} \tag{8}$$

for a differential circuit.

D. Power Dissipation

The power dissipated in the parametric amplifier is only dynamic and is the power required to pull out the inversion charge Q_I from under the gate during the boosting event, as shown in Fig. 11. The energy drawn from the $V_{\rm PULL}$ supply per boosting event is $V_{\rm PULL}Q_I$, with $Q_I \approx C_{\rm ox}(V_G - V_T)$. For a sampling frequency of f_c, there are f_c boosting events per unit time and the theoretical dynamic power is given by

$$P_{\rm diss} = f_c \times V_{\rm PULL}[C_{\rm ox}(V_G - V_T)]. \tag{9}$$

As a typical example, with a sampling frequency of 100 kHz, a $V_{\rm PULL}$ of 3.3 V, a $C_{\rm ox}$ of 2 pF, and a $V_G - V_T$ of 1.5 V, the above relation predicts a power dissipation of 1 μW. Some additional power will be dissipated when charging the junction capacitance.

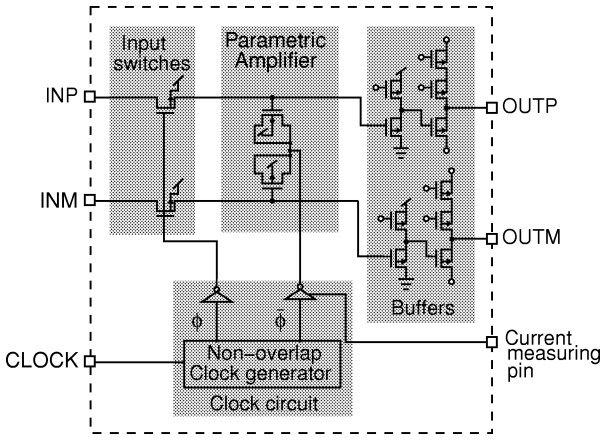

Fig. 12. Schematic of the test chip.

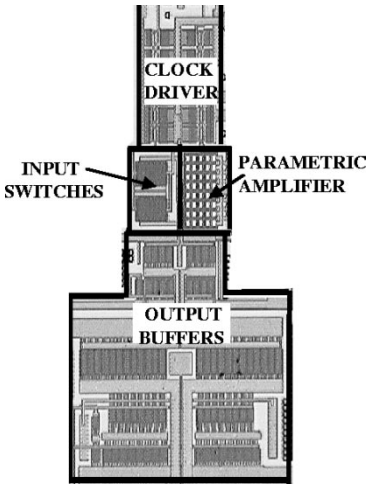

Fig. 13. Layout of the test chip.

III. Experimental Results

A pMOS version of the circuit in Fig. 8 along with supporting circuits was integrated as shown in Fig. 12. The gate voltage as well as the boosting voltage are negative with respect to the bulk, as needed for pMOS devices. The charges on the gates are also negative; this creates positive depletion charges of acceptor ions and positive inversion charges consisting of holes. Thus, a negative voltage $V_{\rm PULL}$ is needed at the source to pull these holes out.

The circuit was designed for low-power low-frequency operation. The size of the transistors used for the parametric amplifier core in Fig. 12 is $20 \times (4.2/4.2)$ μm. A power supply voltage of 3.3 V was used, with the bulk of the transistors connected to this voltage. A clock generator takes an external clock and produces two nonoverlapping clocks used by the parametric amplifier. The ground pin of the inverter that drives the parametric amplifier was used to measure the power dissipated by the latter, including the dynamic power of the inverter itself.

The chip is implemented in a standard CMOS TSMC 0.25-μm process. The chip photograph is shown in Fig. 13. The parametric amplifier can be seen in the center. It was implemented as a bank of unit MOS transistors, to reduce the substrate resistance that appears in conjunction with them in the boost phase.

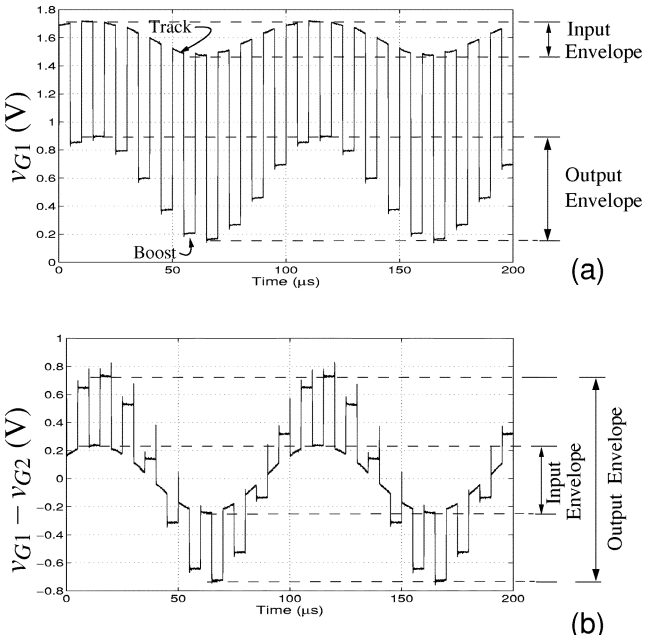

Fig. 14. Measured waveforms. (a) Single-ended. (b) Differential.

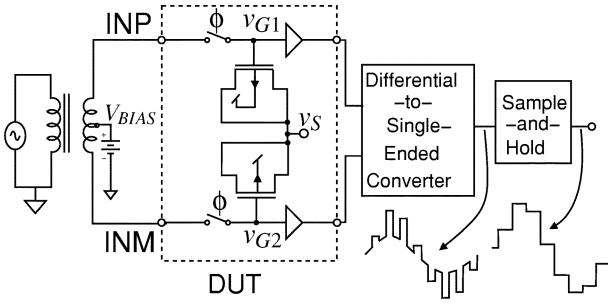

Fig. 15. Distortion measurement test setup.

A. Waveforms

The measured output waveforms are shown in Fig. 14. For this measurement, the hold phase was very narrow compared with the track and boost phases. The single-ended waveform at the gate (a fixed voltage has been subtracted from the buffered outputs in Fig. 12 to eliminate the level shift due to output buffers) is shown in Fig. 14(a). The input is tracked in one phase and the sampled and held value is boosted in another phase, forming the output of the structure. As indicated before, the voltages boost downward due to the pMOS implementation. The input envelope and the amplified output envelope are clearly seen. The measured differential voltage at the output is shown in Fig. 14(b). Again the input is seen in the track phase and the amplified sampled voltage is seen in the boost phase. The voltage gain of the parametric amplifier is 3.1 (at input bias of 1.4 V) and matches with that obtained from SPICE simulation.

B. Distortion

The test setup for distortion measurements is shown in Fig. 15. For measurement purposes, the differential waveform is converted to a single-ended waveform using a differential to single-ended converter. This waveform tracks the input in the track phase and the amplified sampled-and-held voltage

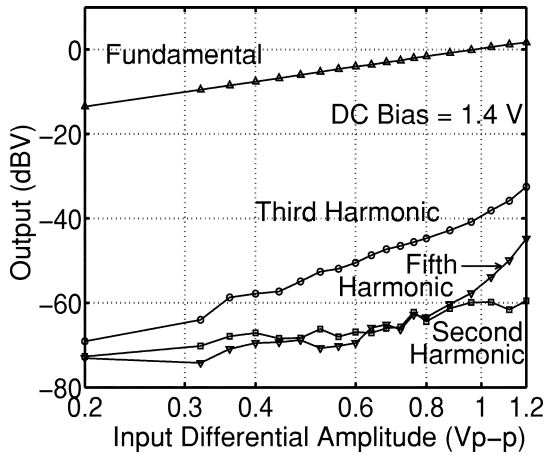

Fig. 16. Distortion as a function of input amplitude.

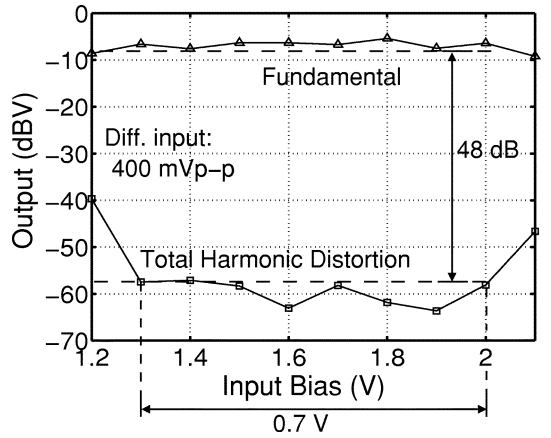

Fig. 17. Distortion as a function of input bias.

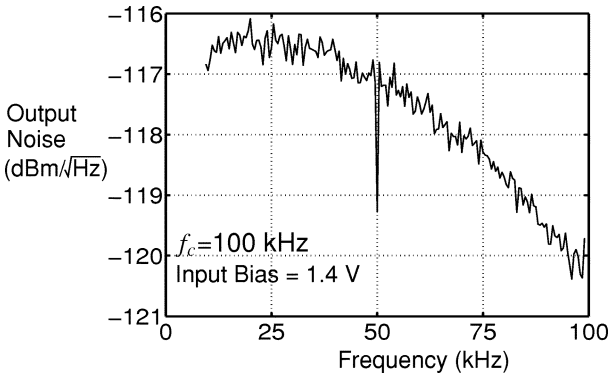

Fig. 18. Output noise spectrum; dBm is defined with respect to 50 Ω.

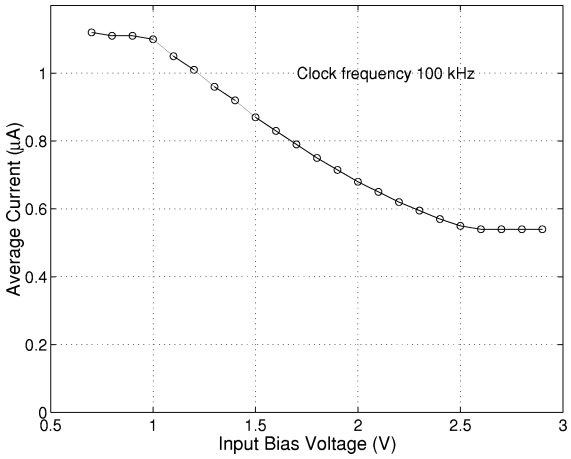

Fig. 19. Measured average current versus input bias voltage.

in the boost phase. A following track-and-hold holds the value of the boosted output for a complete clock cycle. The output waveform is fed to a spectrum analyzer. The frequency response of the measurement setup was calibrated out.

The measured output components are shown in Fig. 16 with respect to the differential input for a bias voltage of 1.4 V. It can be seen that there is good linearity even for large inputs. The second harmonic is also seen to have been substantially reduced due to differential operation.

Since the inversion charge is determined by the bias voltage, it is important to know how the output components vary with the latter. Fig. 17 shows how the fundamental and the total harmonic distortion vary with this quantity. It can be seen that over a bias range of 0.7 V, the fundamental is higher than the total harmonic distortion by over 48 dB.

C. Noise

The measured noise power spectral density is shown in Fig. 18. The total integrated output noise was found to be 4.42×10^{-9} V^2 over the bandwidth from 10 to 50 kHz (measurements below 10 kHz were not used because of the bandpass response of the transformer used to convert the differential outputs to a single-ended output) for 50% duty cycle. This gives an added noise factor of 0.85 dB, in comparison with theoretical noise over the same bandwidth (see Section II-C). An ideal bipolar emitter-degenerated resistively loaded differential amplifier with the same gain, the same linearity, and the same power consumption would give an added noise factor of 2.58 dB. This amplifier would use a total resistance of 3 MΩ due to the low power level used.

D. Power Dissipation

Fig. 19 shows the average current measured through the current measuring pin in Fig. 12 as the input bias voltage is varied. The clock frequency used was 100 kHz. Since the circuit is implemented in pMOS and the bulk is connected to 3.3 V, the higher the input bias voltage the smaller the magnitude of gate to source voltage during sampling and the smaller the inversion charge. This is the reason that the average current drops as the bias voltage increases (see Section II-D). When the bias voltage is close to the supply voltage of 3.3 V, there is no inversion charge in the track phase. The average current thus flattens out to the average current drawn by the driving inverters in Fig. 12.

The plot of the average current with frequency is shown in Fig. 20.

E. Mixing

Subsampling mixers have conversion gains less that 0 dB. In order to restore the amplitude of the signal, an amplifier may be needed following the mixer. The parametric amplifier can be used as the sampling stage instead of using a conventional sample-and-hold with a fixed capacitor. Fig. 21 shows the

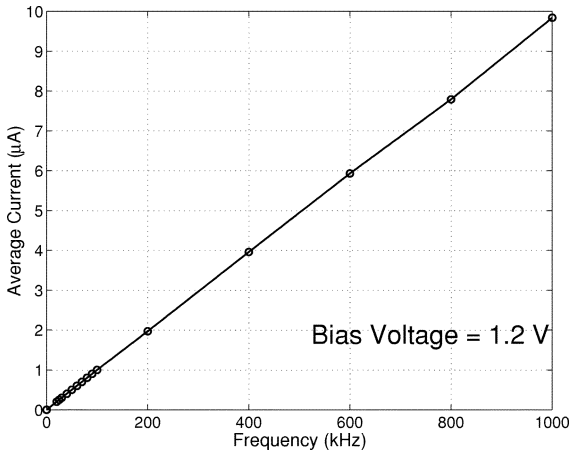

Fig. 20. Measured average current versus frequency.

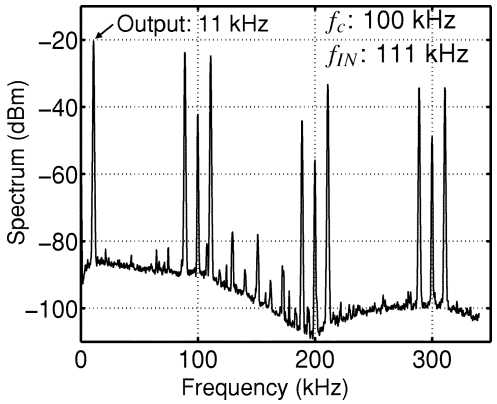

Fig. 21. Output spectrum showing the mixing of input with the clock.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Supply voltage	3.3 V
Clock frequency	100 kHz
Supply current	0.83 μA
Voltage gain (loaded)	3.1
THD (@ 400 mVp-p and 1.4 V bias)	-48 dB
Added noise factor (10 to 50 kHz)	0.85 dB
Input c.m. range for fundamental greater than THD by 48 dB @ 400 mVp-p input amplitude	0.7 V

output spectrum of the differential parametric amplifier with a clock frequency of 100 kHz and an input frequency of 111 kHz. The output contains a component at 11 kHz. The input was at -22.4 dBm and the conversion gain was found to be 2 dB.

The performance summary at a bias voltage of 1.6 V is shown in Table I.

IV. CONCLUSION

Discrete-time parametric amplification based on three-terminal MOSFET varactors have been discussed. Both large-signal and small-signal operation have been considered. Results from a test chip implemented in standard digital CMOS demonstrate low noise due to parametric amplification, very low power dissipation due to zero static current, and large-signal operation with low distortion.

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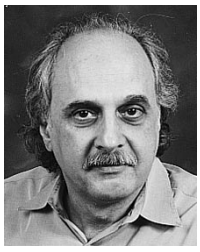

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