Simple Cheap Low Power Oscillators

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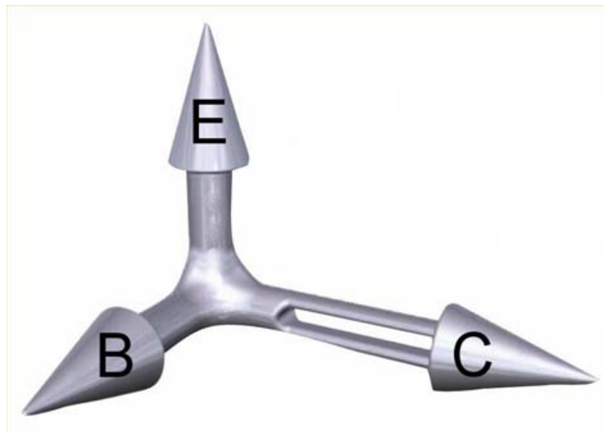
v2.1



INTRODUCTION

Free Energy enthusiasts often require frequency generators or oscillators for their experiments. In some cases a low power design is best suited, especially when attempting to close the power loop with a circuit delivering relatively low output power levels. The purpose of this document is to offer oscillator designs that fulfill this requirement as well as for general purpose needs.

Oscillator designs from CMOS gates are prone to variations in frequency and pulse widths when changing from IC to IC or manufacturer to manufacturer. The circuit builder must keep in mind that these are not precision designs and some tweaking may be necessary to obtain the desired frequency and pulse width (PW) ranges. Use temperature stable timing capacitors (NPO etc.) whenever possible, but it is not critical unless dealing with the tuning of high Q circuits. In this case fine tuning from time to time may be necessary, but automatic frequency control would be ideal, and may be included in a later version of this document.

Circuit design is slightly more complicated when operational amplifiers are involved where single supplies are required. Performance and predictability can be affected if careful consideration is not given to the design. The Sine Wave oscillator designs presented here appear to perform well despite their single supply limitation. With some minor modifications, they can be converted to dual-supply applications.

These are not be-all end-all designs, but are as the title says—simple, cheap and low power. Good performance well into the ultra-sonic range is readily accomplished here. The astute reader will see possibilities for improvements such as output level controls, and frequency range selectors, but for brevity the designs are presented “as-is”, for the moment at least.

This document was inspired by **Ash’s MRA replication** (Panacea University) and the desire to self-power the device. See the overunity forum at: http://www.overunity.com/index.php?topic=6662.0;topicseen

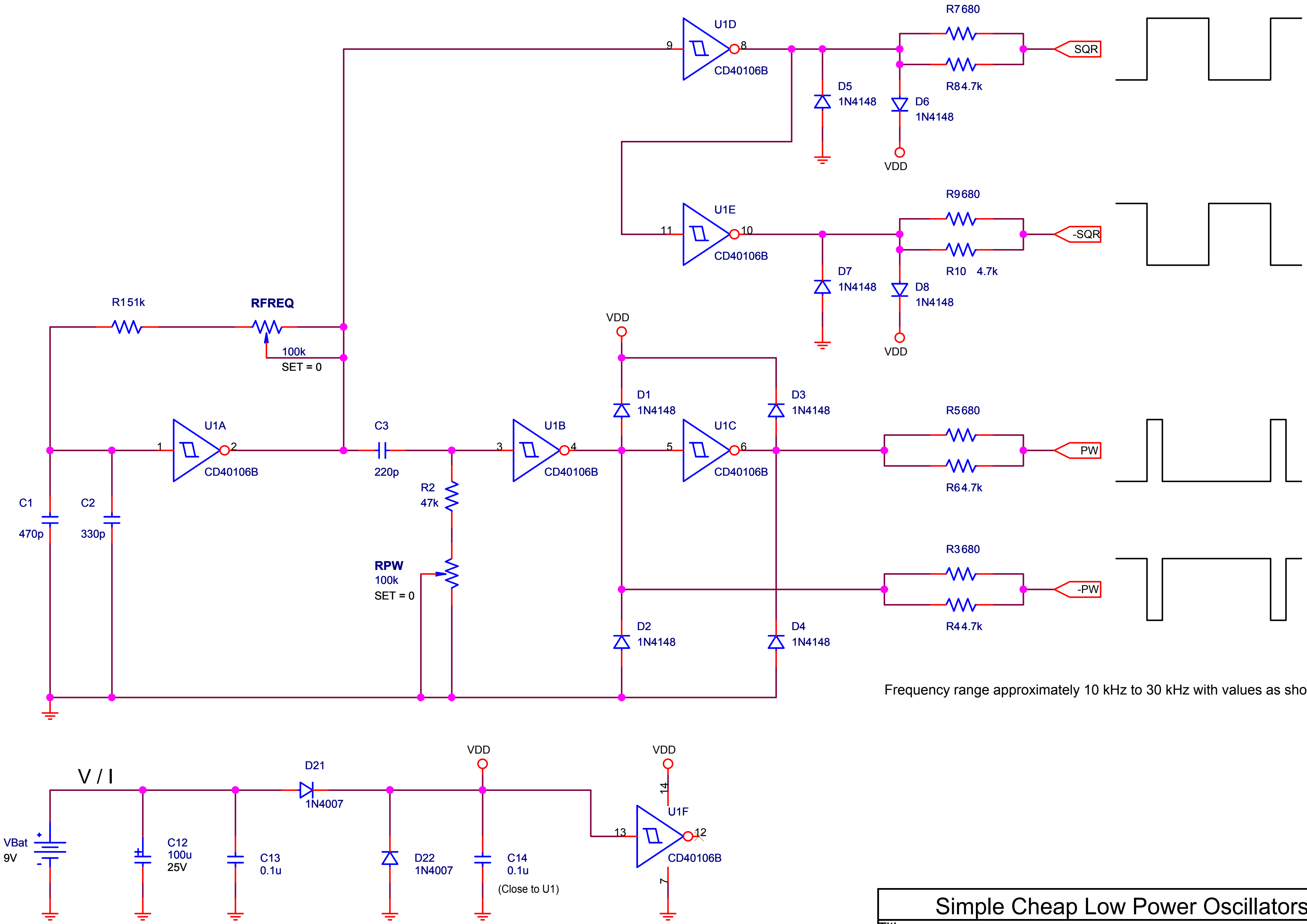
CMOS Square/Pulse Relaxation Oscillator

A very simple low power square wave oscillator is shown in **FIGURE 1** below. Pulse Width outputs are supplied as an option where resonant circuits are driven by the generator. A reduction in the pulse width will result in lower power input. A set of Frequency ranges can be had by switching out (with a rotary switch for eg.) the C1/C2 pair, and pulse width ranges by changing C3. Try log and linear pots for best results.

The capacitor and diode network after the battery are for filtering and protection from transients that may flow back toward the battery, given the pulsing nature of this generator. Any current or voltage measurements should be performed by inserting the meters before D21 where "V/I" is shown in the diagram. This should minimize false readings caused by back-flowing transients into the meters.

Basic Circuit Specifications

Frequency Range ~ 10 kHz to 30 kHz (can be changed by varying R1, C1//C2 and RFREQ)
Pulse Width Range ~ 10us to 50us (can be changed by varying R2, C3, and RPW)
Output Impedance ~ 600 Ohms as shown (optional and can be made to desired)
Output Voltage Swing ~ VOL=0.2V, VOH=8.8V (with a 9V supply as shown)
Power Supply Range ~ 3V to 18V (frequency range may vary with supply voltage)
Power Supply Current ~ 800uA with 9V supply at 30kHz operation (1.6mA for 18V operation)



Frequency range approximately 10 kHz to 30 kHz with values as shown.

Simple Cheap Low Power Oscillators V2.0			
Title: CMOS Square/Pulse Oscillator			
Size: A	Document Number: FIGURE 1		Rev: 1.2
Date: Saturday, February 21, 2009		Sheet 1 of 1	

Wein Bridge Diode Gain Control Sine Wave Oscillator

Sine wave oscillators don't really get much simpler than the Wein bridge type. They use a minimal number of readily available and cheap parts, and perform well considering their relative simplicity. One disadvantage of the design is the need for a dual-ganged potentiometer for frequency control. There are ways to overcome this minor inconvenience but simplicity and minimal current draw is the goal for this first version, so this won't yet be explored.

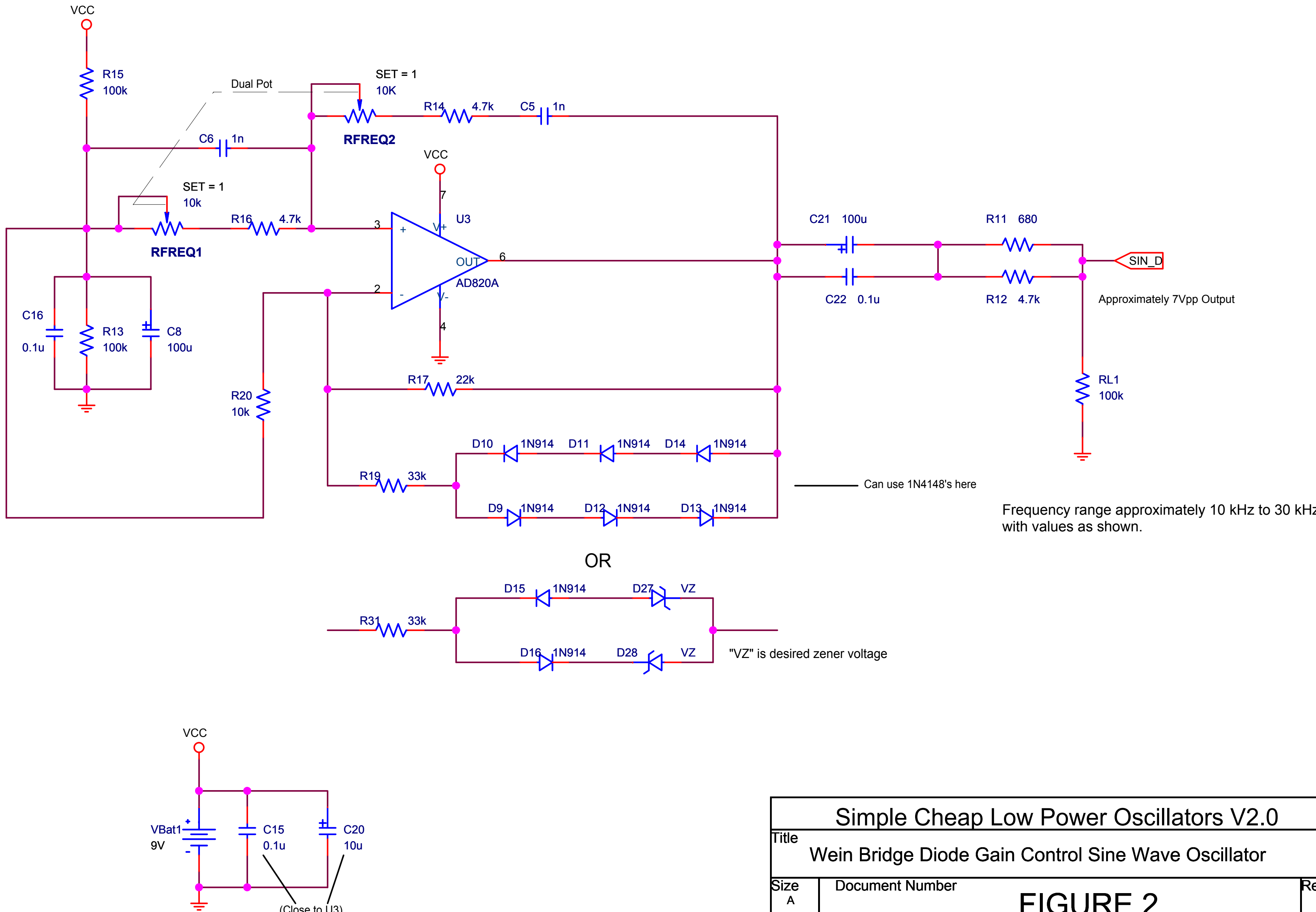
The design uses phase shifts and a balance between negative and positive feedback as a means to achieve oscillation. The phase shift is accomplished with the dual RC network (also the positive feedback portion), and the JFET or diode network controls the amount of negative feedback. The ideal circuit gain is 3, but we start the circuit off with a gain slightly higher than 3 to ensure the circuit begins oscillating. To keep the output from saturating the op-amp, a non-linear gain element is introduced in the negative feedback side which will automatically set the gain exactly to the required value of 3. The output level is set by the threshold at which the non-linear feedback network starts working and this is user adjustable in the sense of setting the maximum peak to peak voltage swing.

In this first design of **FIGURE 2** the negative feedback network is formed by diodes D9-D14 and R19. Three series diodes gave a resulting output swing from about 0.75V to 8.3V with the values shown. If using a supply voltage of 18V it may be more practical to use one diode and a zener in series for each leg, also shown as an alternate.

The number of series diodes or zener value may be changed to accommodate any output voltage level swing. The value of R19/R31 was chosen to give tight amplitude control at the threshold of interest, and it is recommended that this value not be changed. R17 and R20 set the maximum gain of the circuit to about 3.2, and the diode network when in full conduction can reduce it down to about 2.3. After initial startup it will set the overall gain to 3 and remain there.

Basic Circuit Specifications

Frequency Range ~ 10 kHz to 30 kHz (can be changed by varying the RC network values)
Output Impedance ~ 600 Ohms as shown (optional and can be made to desired)
Output Voltage Swing ~ VOL=0.75V, VOH=8.3V (with a 9V supply as shown)
Power Supply Range ~ 5V to 36V single supply
Power Supply Current ~ 1mA



Simple Cheap Low Power Oscillators V2.0		
Title: Wein Bridge Diode Gain Control Sine Wave Oscillator		
Size A	Document Number: FIGURE 2	Rev 1.0
Date: Saturday, February 21, 2009	Sheet 1 of 1	

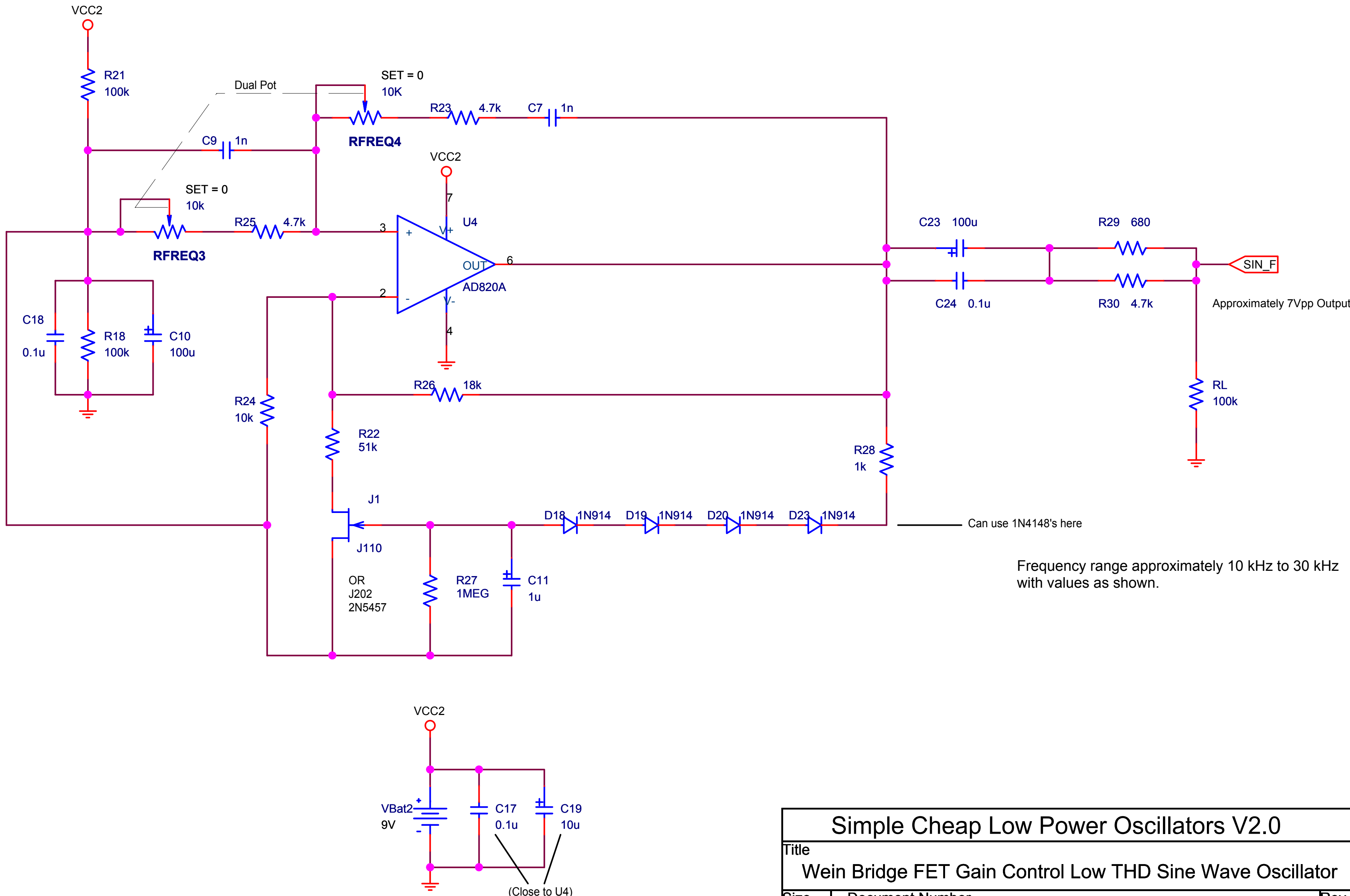
Wein Bridge FET Gain Control Low Distortion Sine Wave Oscillator

A lower distortion version of the Wein bridge oscillator is shown below in **FIGURE 3**. The non-linear amplitude control element in this case is a JFET device. The principle is the same as in the diode control version, but the JFET is a normally “ON” device, so it is placed in the shunt leg of the feedback network. Here it begins to reduce the gain when its negative Gate drive increases. Initially the JFET places R22 in parallel with R24 giving an overall circuit gain of about 3.15, which is enough to elicit oscillation. As the output amplitude grows the op-amp may saturate briefly until the buildup of Gate voltage exceeds the JFET’s V_{GS}off, at which point the gain will be reduced and settle at the required value of 3.

Three different JFET types were tried and are specified on the drawing. No other part value changes are required. As with the diode gain control version, the number of series diodes with the Gate will set the peak to peak output voltage swing, so if changing to a higher supply voltage (up to 36V), it would be prudent to take advantage of the extended output swing, if desired. Use a series zener plus one diode if desired output levels become high. The R28 1k resistor is used to add a small attack time to the gain control to ensure the circuit starts oscillation.

Basic Circuit Specifications

Frequency Range ~ 10 kHz to 30 kHz (can be changed by varying the RC network values)
Output Impedance ~ 600 Ohms as shown (optional and can be made to desired)
Output Voltage Swing ~ VOL=0.55V, VOH=8.3V (with a 9V supply as shown)
Power Supply Range ~ 5V to 36V single supply
Power Supply Current ~ 1mA



Simple Cheap Low Power Oscillators V2.0		
Title: Wein Bridge FET Gain Control Low THD Sine Wave Oscillator		
Size: A	Document Number: FIGURE 3	Rev: 1.0
Date: Saturday, February 21, 2009	Sheet 1 of 1	

APPENDIX 1 – Closing the Loop (is COP >1?)

With a working DC-powered oscillator driving an overunity device, it should be possible to close the power loop and determine if the observed output power is greater than the input. One simple way of achieving this test is to configure the system per the diagram below.

The only requirement for this simple scheme to work is that the output voltage VOUT be greater than the battery voltage VBAT.

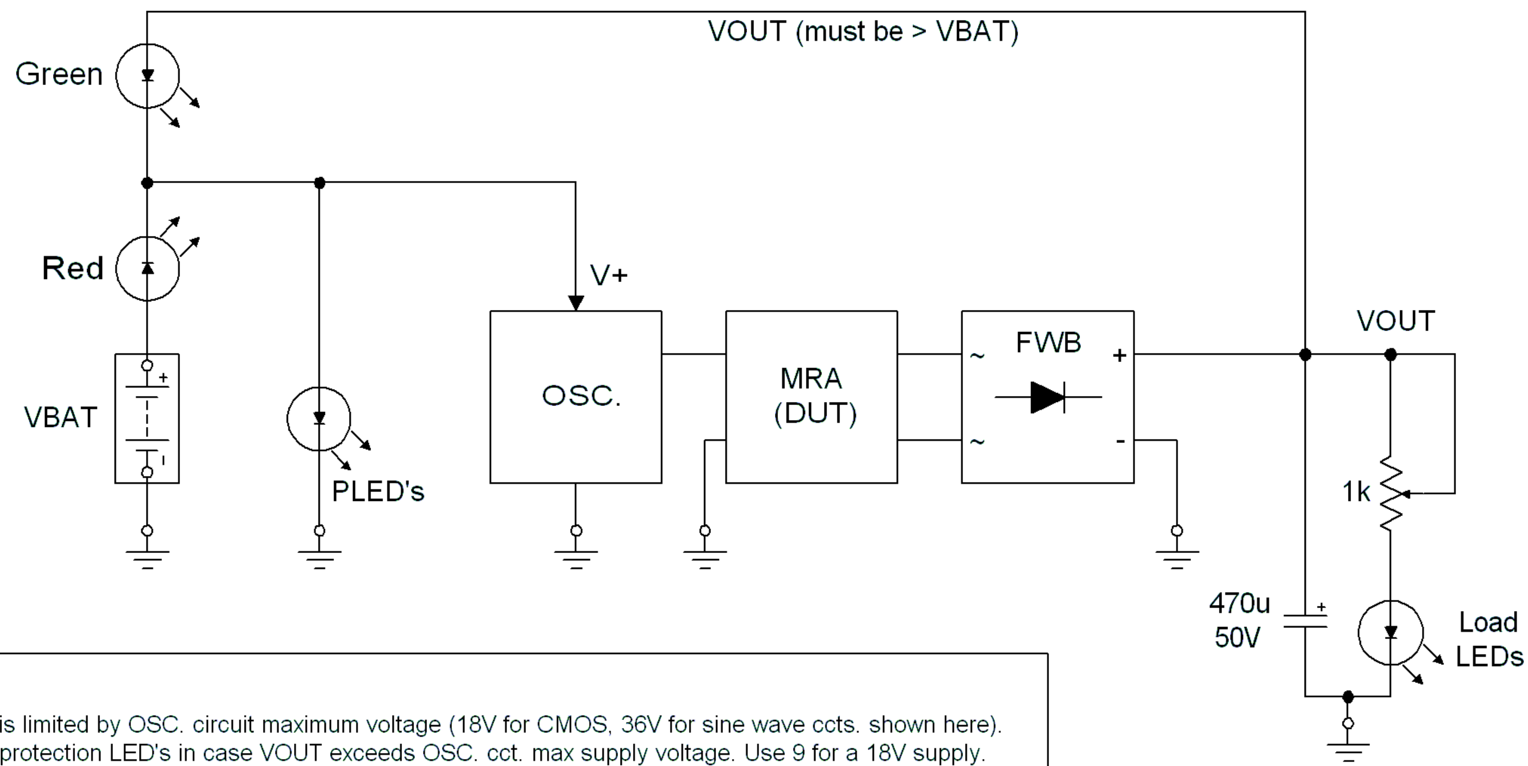
The MRA is shown as the overunity device, but this setup can be used for any device that uses a drive input frequency to obtain a final DC output voltage greater than VBAT.

If the device under test (DUT) is in fact achieving overunity, the setup will self-run under its own power because of the diode isolation from the battery. The battery can be removed if after startup, the Green LED is ON. If the DUT is underunity (single Red LED ON, and Green LED OFF), the battery will eventually drain and the circuit will stop operating.

The PLED's connected to V+ are for protection in case VOUT exceeds the OSC. circuit maximum operating voltage. They will provide more load (and light) to the DUT at this point. However, they may not be necessary if under load from the "Load LEDs", VOUT does not exceed this maximum limit. Adjust the number of "Load LEDs" and the 1k pot setting as necessary. Ensure Load LED current does not exceed 20mA.

Start by using a 10k resistor in place of the Load LED's. Measure VOUT. Adjust the supply voltage and the number of LED's appropriately. Try to keep VBAT and the OSC. circuit VPP close in value.

Simple Cheap Low Power Oscillators - 10



Notes:

1) VBAT MAX is limited by OSC. circuit maximum voltage (18V for CMOS, 36V for sine wave ccts. shown here).
2) PLED's are protection LED's in case VOUT exceeds OSC. cct. max supply voltage. Use 9 for a 18V supply.
3) Begin by using a 10k resistor for the load (i.e no Load LED's), and measure VOUT. Set the number of PLED's and Load LED's accordingly.
4) Try to keep VBAT close to the OSC VPP output. Using too high a value for VBAT and not compensating to increase the OSC. cct. VPP output voltage might nullify the chance to achieve COP>1 operation.

"Closing the Loop" Setup – is COP >1?